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On-Chip Spectral Analysis for Built-In Testing using FFT Engine

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Abstract: On chip Built in testing of electronic equipment is very much necessary these days this is because customers are demanding more value for their money spent on electronic gadgets. The accurate and efficient analysis requires use of a very precise hardware and software. Also full understanding of test signals and system is required to perform spectrum analysis. FFT(Fast Fourier Transform algorithm) is the technique which can be used to perform built in test and calibration with the help of multi tone test signals with certain inter modulation component and harmonic component. To increase the accuracy of algorithm it I required to use large no of FFT test points. But if we increase FFT points the it will result in power consumption and large area this difficulty can be overcome by using coherent sampling rather than using traditional sampling method.

I . INTRODUCTION

An important concern of IC manufacturers is the Efforts required to implement BIST on their Chips. The objective of the manufacturer is to build and sell the IC at a profit. If BIST is not used at all, then there will be no overhead at all in the manufacturing, however, more sophisticated equipment will be required for each test, and repair will be more costly due to the increased difficulty of diagnosing any problems. Integrated calibration[1] and digital based analog circuit[5]design methods are becoming popular these days . The performance parameters and characteristics of circuit to be tested can be observed by output spectrum. Which led to on chip spectrum analyzers, which will emulate off chip system [2]. It is also proposed that ADC and DSP resources should quantize the analog signals of circuit for computation of FFT and tuning with DAC[3].

The FFT algorithm can be applied to a particular block or to series of blocks. The test signal frequency to be used always depends on clock frequency of FFT and sampling frequency. Effective calibration always requires sequential injection of test signal frequencies at various test points of FFT which can be accomplished with switches[4]. Consider an example, we have two test tone frequencies f_1 and f_2, then by monitoring spectral components of the circuit under test we will be able to determine 3^{rd} order characteristics. If the sampling frequency should be low then (f_2-f_1) can be assured to be low by selecting correct test tone frequencies.

The FFT is one of the most commonly used digital signal processing algorithm. Recently, FFT processor has been widely used in digital signal processing field applied for communication systems. FFT processors is key components for an Orthogonal Frequency Division

Multiplexing (OFDM) These requirements typically translate into a large number of FFT points resulting in area and power requirements. The purpose of the proposed FFT approach is to reduce the overhead associated with on-chip FFT implementations for built-in testing.

II . FFT ALGORITHM

The original FFT algorithm was designed for calculation of input waveforms of a spectrum only for certain frequencies which are separated from fundamental frequencies (F_f). The F_f depends on the sampling frequency f_s as wel as NFFT, where N denotes length of FFT such that

$$F_f = f_s / NFFT$$

To reduce the spectral leakage and for frequency resolution we can reduce f_s or FFT length can be increased, but we have constraint on sampling frequency and this constraint is that it should satisfy niquist criteria butw e can not play with f_s while dealing with on chip analysis. However if we increase the length N of FFT it increases the area and feasibility of FFT algorithm in testing. Thus FFT algorithm is merely useful in multi-tone testing because of spectral leakage problem.

One technique is useful inand efficient for on chip spectrum analysis [6] and the technique is coherent sampling [7] . Condition for oherent sampling is given by

$$f_i/f_s = N/NFFT \text{……..(1)}$$

Where f_i is the input frequency, f_s is the sampling frequency, N is no of cycles to be sampled and NFFT is length of FFT. Coherent sampling is generally used in single tone testing. This is because input frequency can be calculated for single frequency component.

III. PROPOSED TECHNIQUE

Proposed approach is based on coherent sampling as mentioned in the above section. The sampling frequency is chosen on the basis of frequency difference between the tones in multi-tone test. But before going toward our main aim that is multi–tone test we will first discuss single tone test.

The sampling frequency equation (1) is rearranged and given by

$$f_{sc} = f_i*NFFT/N \text{…….(2)}$$

in this case f_{sc} is coherent sampling frequency which is calculated for required input test frequency f_i for FFT length NFFT and number of cycles of input test signal.
However for performing multitone test the fundamental frequency is ∂f and it is used in calculation of f_i in equation (2). In multitone test the spacing between the test tones should be equal to ∂f or multiples of ∂f. With predefined value for ∂f the corresponding value of f_{sc} can be determined as follows

$$f_{sc} = \partial f*NFFT/N \text{……..(3)}$$

The choice of test tone frequency is chosen as follows
a) The test tone frequency should be integer multiple of ∂f
b) The test tone signal frequency should be less than half of $f_{sc.}$
If test frequency is chosen by following the above criteria we will be able to eliminate spectral leakage but also we will be able to achieve certain benefits such as

a) Spectral characteristics can be determined for obtaining higher order harmonics of input test tone signal.

b) Spectrum of input frequency f_i and its harmonic can be accurately calculated without aliasing and spectral leakage up to seventh order.

c) The noise levels with our approach is generally low.

As a reference for comparison to the post-layout 16-point FFT results, the "Calculated Input" columns include the corresponding frequency component values obtained for the same input with an ideal 65 536-point FFT. An error of less than ±0.02 dB is observed for the fundamental components at 3 and 5 MHz, whereas the applied 50-dBc IM3 components at 1 and 7 MHz are captured with an error of 0.72 and 1.32 dB, respectively. The post-layout FFT engine simulation results indicate that the chosen combination of a 10-bit ADC and a 16-point FFT in this example is suitable to accurately determine the IM3 components of ≤ 50 dBc.

IV.CONCLUSION

An accurate FFT-based analysis approach was introduced for on-chip spectral characterization of multi-tone signals. The proposed approach was derived from the coherent sampling method. It was demonstrated using VHDL that it allows the designer to select the appropriate test signal frequencies, ADC resolution, and FFT length to achieve the desired frequency resolution in the output spectrum without spectral leakage. The method avoids the use of a large number of FFT points to minimize the required on-chip FFT resources for area- and power-efficient built-in testing applications For a 16-MHz 16-point FFT computation, the implemented FFT engine consumes an estimated power of 5.57 mW with 1.1 V supply and occupies an area of 0.068mm2. A methodology was presented to determine the suitable ADC resolution and the FFT length to obtain a required accuracy. For example, when combined with a 10-bit ADC, the simulated error for IM3 extraction from the output spectrum of the 16-point FFT is within 1.5 dB for IM3 components ≤ 50 dBc.

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