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DESIGN FLOW FOR CLOCK LOAD REDUCTION IN FLIP-FLOP'S USING CPSFF

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Abstract

Clock Gating logic is generally in the form of "Integrated clock gating" (ICG) cells. For reduce the dynamic power dissipation the popular technique which could be used as Clock gating. In flip-flop the switching state consumes high power. When not being switched, the switching power consumption goes to zero, and only leakages current are incurred. To reduce this power Clock gating technique adds some more logic to the circuit to prune the clock in the circuit. This technique save the area and also the power to reduce the N number of transistors and the MUX by replace the clock gating logic circuit. The clock distribution network (CDN) provides the clock to the logic circuit having the common point. Also the circuit which could be having the CDN consumes the large amount of power being processed in high frequency of operation. An efficient way to reduce this effect the capacity of the clock load is to become less which is having minimum number of transistors. Hence we are proposing the novel approach as Clocked load shared Flip-flop (CPSFF) to reduce the Clocked transistor. The performance of this proposed Circuit has been verified by using the DSCH and MICROWIND tool in layout and power consumption level.

Key words: clock gating, CPSFF, clock load.

Introduction

The clock signals are to be enabled at the process of system level and it can be effectively capture the functional block modules. This could be need not be clocked. These signals are activated later into the clock enabling signals in the form of gate level. In the other devices the clock signals are automatically added by the design consideration. Still, the circuit having some floating at the high level. For this situation we need to calculate the dynamic power consumption consumed by a circuit when the clock signals are enabled. This period is assessing the clock gating requires the analysis and the requirements of FF's Pre-charge and evaluation state as presented.

The clock will be disables in the next cycle by XOR-ing the output of the present data input and it will reveal at the output in the next cycle. Then the output of the XOR gates are OR-ed for generating the gate signal for the FF's which is to be used to avoid the glitches. The Integrated clock gate (ICG) can be used by the environmental tools by the combination of LATCH with the AND gate [13]. These latches could be used in ultra low power applications for a digital filter. The data driven clock gating signal are being used as an enabling signals in this applications. There will be a trade off for ICG is the number of clock pulses could be disabled. The pulses could also be a tradeoff for the hardware overhead. While increase the number of flip-flops the hardware overhead decreases to obtain by OR-ing the enable signals. The level of this high and the low state of signals could be processed in the same versa to give the proper output.

The clock gating signals are not enable as free. The logics and the interconnections are could be desired to enable those signals and the output can be covered by area and the power consideration. In some operation individual clock input has been given to the FF's and it consumes more amount of power. These clock separations have been yielding more size also. This could be results in high overhead of the output. Thus the clock load has been reduced by using the circuits shared by Flip-Flops. This could be consumed small amount of power.

The registers attached to use the clocks and the enable condition used by clock gating. To achieve the clock gating from the enable conditions in order to use the imperative design. This process also save the power as well as large number of MUX's in the logic circuit. These circuits are could be replaced by using the Clock gating signals from the CDN. The general form of the ICG can also to be distributing these signals to the clocks for the level of interchanging as a part of the CDN. Since the level of the clock gating logic change the clock tree structure and it will be remain at the same tree.

Clock gating logic levels having the strategy are as follows:

1) The RTL level code has to enable the condition which could be accessed the logic level synthesis.
2) The design could be specific modules or a registers that can be processed by ICG as a library function.

3) The automated clock gating has been semi-automatically inserted and it will be generated as an ICG cells. So this will be enable the RTL level or it will be insert into the ICG level for the optimizations..

Existing System

Conventional CDN with sequential elements

In the conventional flip-flop's the CDN can having the sequential elements like flip-flop's and latches. The clocking system which could be distributing the clock signals to the elements having the high power consumption along with the N number of clock signals. The load for the clock signals has been additionally added and it will produce the individual clock system to the circuits. In a VLSI system this could be a major concern for designing the circuits. The high power has been consumed by the clock drivers for the fabrication of on-chips. For the single edge triggered flip-flops and the transmission gate flip-flops are having master and slave.

For this type of flip-flops is also having the two stages while its operation, it reaches the output stage having higher time consumption. So this leads to higher power consumption for the circuit and also the layout level of consideration. The switching delay are increased by using the CDN flip-flops contains N number of clocking transistors. The description of this delay has to be modified as a level of the transistor size and the level of the clock load. This state of the pre-charge and evaluate can also be derived in the circuit as a layout and the debugging level. This level modified as the CDN elements for the external signals which could be enabled as a part of the other consideration for the clock pulses. These gating cannot be added as a signal generation for the adopted level to their signal level modification.

Proposed System

Clock gating technique

In flip-flop the clock load is main concern for consuming the power as dynamic dissipation. The clock gating is a popular technique that could be evaluated to reduce the power consumption in the designed circuit. The related features as area and also the performance get declared as a form of energy into the designed circuit. The signals can be enabled by the sector to the level of layout and the area. Sequential clock gating is used to enable the up and down streams for the extracting process. For this enable conditions the additional registers can be clock gated. By the asynchronous circuitry the various clock gating can be defined by the "clock" for simple approximations of the data-dependent exhibited circuit. As we can gate this synchronous circuit the clock enabling signals are get extracted and then it goes to zero for the power consumption in that circuit. This circuit only enables the condition which could be allocated at the logic level transitions and the process of getting the output data for these enabling signals.

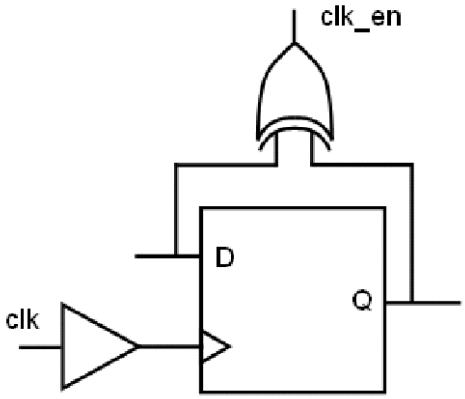

Figure 1. Clock signal enabling

The enabling signal EN cannot be supplied to the circuit means it does not supply the clock pulses. When this type of situation get communicated the power dissipation can be saved as a register and more circuits. The reason can be eliminating the signal which could be transferred to the inputs of the registers and the dynamic power dissipation can be saved if clock pulses are not enabled. But this situation can be continued means the performance of the circuit and that the portable device cannot be in the form good performance for these signals. The way cannot be handled in that term to the registers for the signal transitions for this fan-out condition to be eliminated.

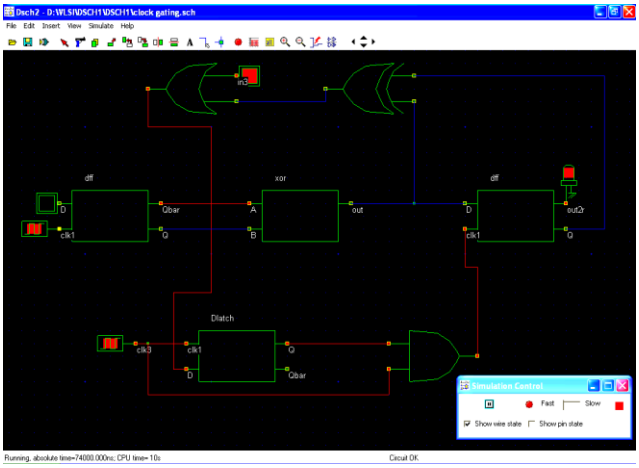

Figure 2. Schematic for clock gating

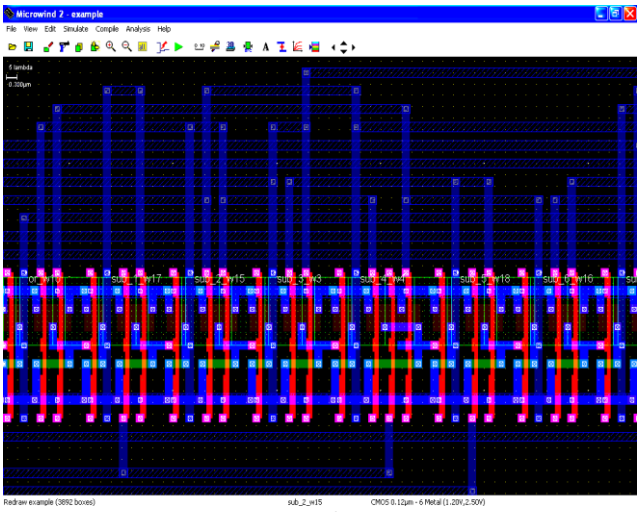

Figure 3. Layout for clock gating

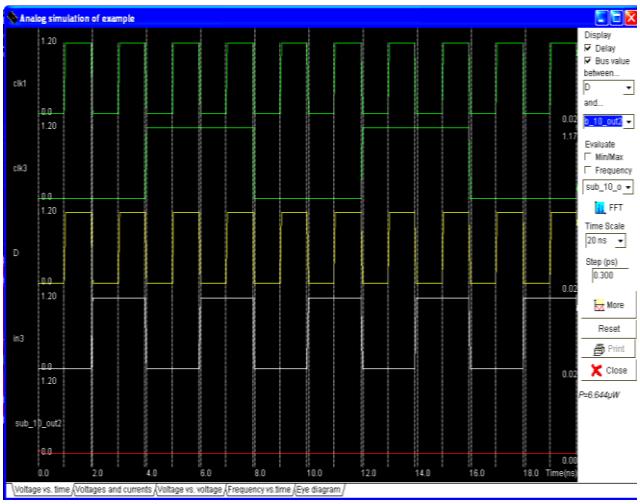

Figure 4. Waveform for clock gating technique

Clock load reduction by using CPSFF

In the electronic circuits clock load has been a major concern for the system development and the chip manufacturing process. It could be heavily limited by using the Clocked pair shared flip-flop (CPSFF) technique. This technique has been widely used in circuit designing for the all flip-flop as CDN elements. The portable electronic devices are under this manufacturing process its getting low dynamic power consumption. This will be revealing the purpose of the system that could be considered as a part for the relevant design process for the all CDN network in the sequential circuits.

So when the power consumption becomes dramatically reduced, the heat dissipation will be limited the performance of the VLSI circuits and systems. In data control path the flip-flops and the latches are synchronous from the current design in this way. The major challenge in the VLSI low power system is the power dissipation in the sequential elements. For non-affecting the system of the sequential elements we have to perform the operation when we need to be reduce the power consumption.

So, this switching activity could be reduced and it will be generate the performance for the related sequential elements. There are two ways to reduce the switching activity: 1) conditional operation by used to eliminate the redundant data switching.2) clock gating by used to reduce the clock also. This conditional level operation could be performed as a particular scheme when we get the same output as to compare with the power consumption. The conditional operation could be in the internal node for the capturing level of the flip-flop. For this, when the input level stays in the logic one level, this internal node getting charging and also discharging without using the computation format.

In clock gating, we can have the certain level of operation to be performed as a clock signal to save the power consumption. So by using the conditional and the clock gating level is used to reduce the power by decrease the switching activity.

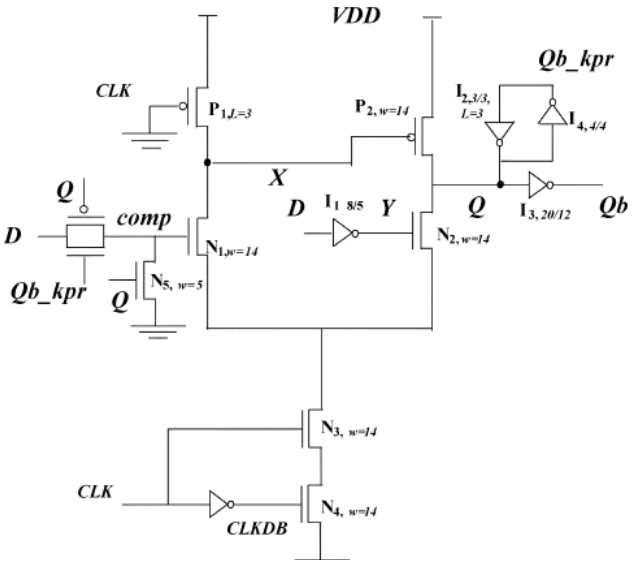

Figure 5. Circuit for CPSFF

In the CPSFF (Clocked-pair shared flip-flop) clocked pair i.e (N3, N4) is shared between the first and second stage of the circuit when it could be converted as a signal level of combination. The P1 is used to charge the internal node of the P-MOS by using the pre-charged transistors as (P1, P2) in the pair of the flip-flops. Compared with this circuit description to the conditional mapping flip-flop the clocked transistor size could be reduced. According to this the clock load has been decreased as much as compared to the other conventional circuits. This circuit could be an efficient design to the external node of the transistor level. Further the N7 could be in the conditional mapping was removed as a reduction of the transistor size in the CPSFF. By using the four clocked transistor by replacing the conditional mapping level that could be heavily limited the power consumption criteria. The resulting level of this transistor output is heavily as much as compared to the conventional as 40% of the proposed system.

When we give the data input as D=1, Q=0 and Q bar=1 and then the related transistors N5 and N1 will be turn OFF and the voltage will be passed through N3 called as ground voltage. That will be pulls up the ground voltage through P2 and then it will be turn OFF. This section cannot be access as a transistor in the sequence of the voltage drop. Then for the opposite condition for this flip-flop this signaling level could be enabled and the output will be obtained from the data input. For this operation the data will be handled as 1 and then the transistor N2 will be OFF and the N1 is ON. Then the output pulls down to zero through the transistor as N2. Then the related flip-flop output could be depending on the previous output of the Q and Q bar in the additional level of the clock and the data input. This level will be across to the previous state of the section as required in the section of the data. This will be reset as a level for the created output of the particular data input. Whenever the Transmission gate of the input is always high the output transistor will be enabling. The data and the clocked transistor level in the sectional output become low.

To reduce the existing system circuit power consumption in proposed flip-flop, the output of the flip-flop always depends upon the previous stage of the flip-flop output. For this condition without giving the removal of noise pulses in the coupling of transistors, we give the initial conditions of the flip-flop. The double-edge triggering flip-flop for applying the real time version of the proposed flip-flop is to be cleared from the noise level of the existing circuit. So the proposed level circuit will give the output power consumption as very less when compared to the conventional flip-flops.

Simulation Results

The CPSFF circuit could be drawn by using the DSCH tool and verified as by the level of the section in the designed circuit. The layout and the compilation could be verified using MICROWIND. By the level of this consideration we could find out the output as the power consumption of the proposed circuit. This design could be analyzed as the circuit in the proposed design.

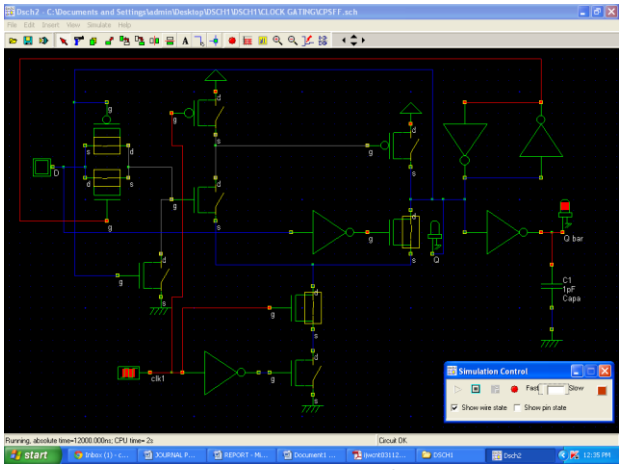

Figure 6. Schematic level for CPSFF

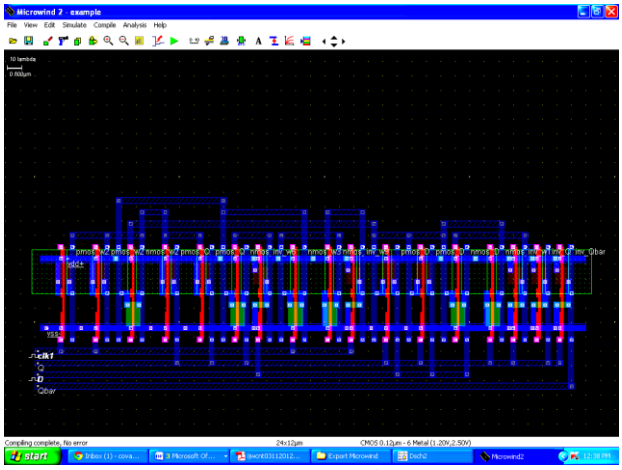

Figure 7. Layout level for CPSFF

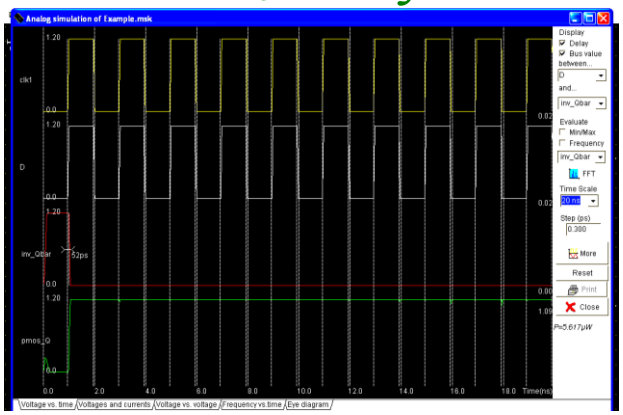

Figure 8. Waveform for CPSFF

Conclusion

In this paper the low power design methodology and the low power flip-flop design could be drawn and verified by using the DSCH and MICROWIND. The combinational and the sequential circuits for the low power applications is more importance for the area of research in circuit designing. Here we are analyzed about the low power flip-flop applications and we present a survey regarding this application. Our experimental results are to be used to analyze the existing flip-flop designs by the way of power leakage. This could be considered and followed by this proposed design to implement this survey and the evaluation of the circuits. The performance of the proposed design could not be limited as much in the conventional circuits.

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Biography

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