ISSN:2321-1156
International Journal of Innovative Research in Technology & Science(IJIRTS)

Area and Power-Efficient Carry Select Adder

Laxman Shanigarapu
Dept. of ECE
MANIT, BHOPAL
laxmanbits83@gmail.com

Bhavana P. Shrivastava
Dept. of ECE
Ast. Professor, MANIT, BHOPAL
sonibhavana1@gmail.com

***Abstract*— Adders are the basic building blocks of any processor or data path application. In adder design carry generation is the critical path. To reduce the power consumption of data path we need to reduce Area of the adder. Carry Select Adder is one of the fast adder used in may data path applications. The proposed design is implemented without using multiplexer and RCA structure with Cin=1. Instead of multiplexer and RCA Cin=1 structure hear we used simple combinational circuit which consists AND and XOR gates. In this proposed design has reduced Area and power as compared with regular CSLA and modified BEC(Binary to Excess-One Converter) CSLA with slight increase in the delay. In this proposed design power and area is reduced to 47.7% and 54.5% for 8bit, 48.3% and 52.76% for 16bit, 49.65% and 52.9% for 32bit, 49.7% and 51.56% for 64bit when compared to the Regular Carry Select Adder (CSLA). Power and area is reduced to 44.08% and 30.8% for 8bit, 44.9% and 30.07% for 16bit, 45.39% and 30.3% for 32bit, 44.9% and 29.56% for 64bit when compared to the modified CSL adders (BEC).**

Keywords- CSLA, COMBINATIONAL CIRCUIT, BEC, LOW POWER.

I. INTRODUCTION

Design of area and power-efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use simple combinational circuit instead of RCA with cin = 1 and multiplexer in the regular CSLA to achieve lower area and power. The main advantage of this paper is logic comes from low power than the n-bit Full Adder (FA) structure. The details of this paper are discussed in Section VI. This brief is structured as follows. The SQRT CSLA has been developed by using simple combinational circuit and compared with regular SQRT CSLA and ref[4].

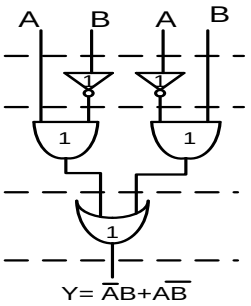


Fig.1 delay and Area evaluation of an XOR gate

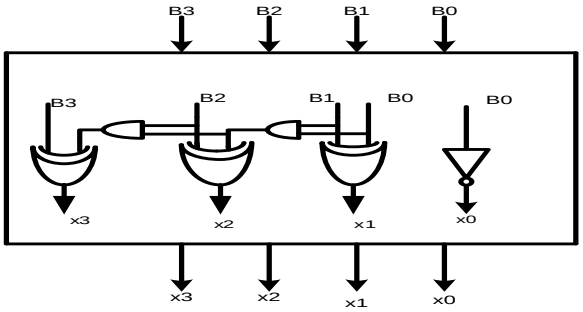


Fig.2 4-bit BEC(Binary to Excess-One Converter)

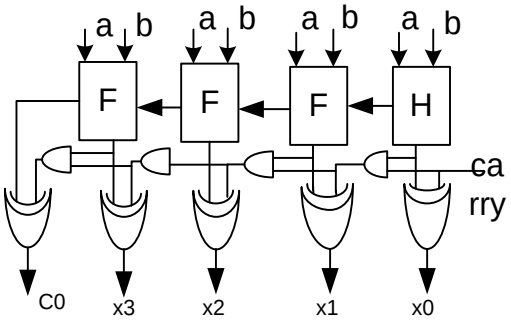


Fig.3 4-bit CSLA Without using Multiplexer

Fig.1 shows the internal structure of XOR gate which consists 5 gate and 3 gate delays. Fig.2 shows the internal structure of the 4-bit BEC (Binary to Excess-One Converter) which converts binary number to excess-one. Fig.3 shows the 4-bit CSLA without using Multiplexer. The RCA structure cin =0 output is given to the combinational circuit which consists XOR and AND gates it will calculate the output without using RCA cin = 1 structure and multiplexer.

II LITERATURE REVIEW

Bedriji 1962 proposes that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums.

AkhilashTyagi 1993 introduces a scheme to generate carry bits with block carryin 1 from the carries of a block with block carryin 0.

Chang and Hsiao 1998 propose that instead of using dual carry ripple adder a carry select adder scheme using an add one circuit to replace one carry ripple adder.

Youngwood Kim and Lee Sup Kim 2001 introduces a multiplexer based add one circuit is proposed to reduce the area with negligible speed penalty.

Yajuan He et al 2005 proposed an area efficient square root carry select adder scheme based on a new first zero detection logic.

Ramkumar and Harish 2012 propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

Padma Devi et al 2010 proposed modified carry select adder designed in different stages which reduces the area and power consumption.

III. DELAY AND AREA EVALUTION METHODOLOGY OF THE BASIC ADDER BLOCS

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. Then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

TABLE I

DELAY AND AREA COUNT OF THE BASIC BLOCKS OF CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

As stated above the main idea of this work is to use simple combinational circuit instead of the RCA with cin=1 and multiplexer in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n-bit combinational circuit is required. A structure and the function table of a 4-b combinational circuit are shown in Fig.3 and Table II , respectively. Fig.3 illustrates how the basic function of the CSLA is obtained by using the 4-bit combinational circuit without using mux. The importance of this method is logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

TABLE II

Function Table Of The 4-bit Without Using MUX Circuit

B[3:0]	Carry=0 X[3:0]	Carry=1 X[3:0]
0000	0000	0001
0001	0001	0010
0010	0010	0011
:	:	:
:	:	:
1110	1110	1111
1111	1111	0000

The Boolean expressions of the 4-bit without mux circuit is listed as (note the functional symbols ~ NOT, & AND, ^ XOR)

X0 = B0 ^ CARRY

S0 = B0 & CARRY

X1 = B1 ^ S0

S1 = B1 & S0

X2 = B2 ^ S1

S2 = B2 &S1

X3 = B3 ^ S2

IV. Delay and Area evaluation of REGULAR 16-B SQRT CSLA

CSLA compromise between Ripple Carry Adder and Carry Look Ahead Adder. When compared to RCA CSLA is high speed and when compared to Carry Look Ahead Adder hardware complexity less. The main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The Fig.4 shows the regular 16-bit carry select adder. It is divided into five groups with different bit size RCA. Internal structure of the group 2 to 5 of regular 16-bit CSLA is shown Fig.5. One input to the multiplexer goes from the RCA with Cin=0 and other input from the RCA with Cin=1. Finally multiplexer gives the proper output.

TABLE III

Delay And Area Count Of Regular SQURT CSLA Groups

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

Table III shows the delay and area count of the regular CSLA. There is a chance to reduce the area, power and delay in the CSLA structure.

V. MODIFIED 16-B SQRT CSLA (BEC)

The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The modified16-bit CSLA using BEC is shown in Fig.6 Ref [4]. The structure is again divided into five groups with different bit size RCA and BEC. The group 2 to 5 of the modified 16-bit CSLA is shown Fig.7. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 to 5 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power But there is a slight increment in delay.

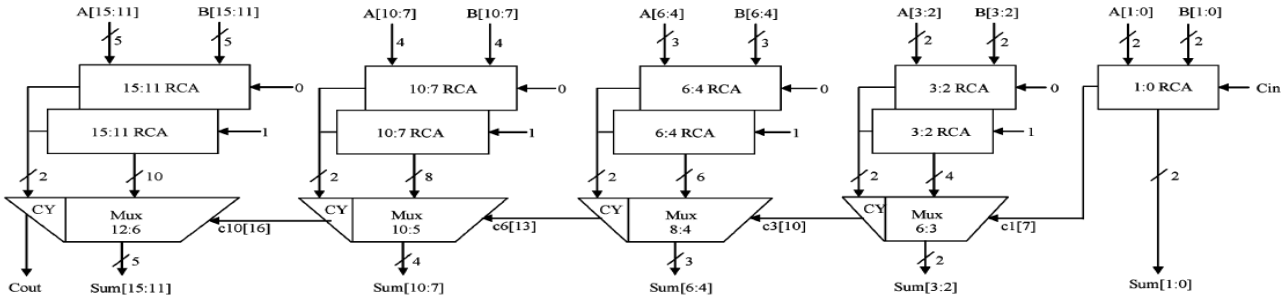
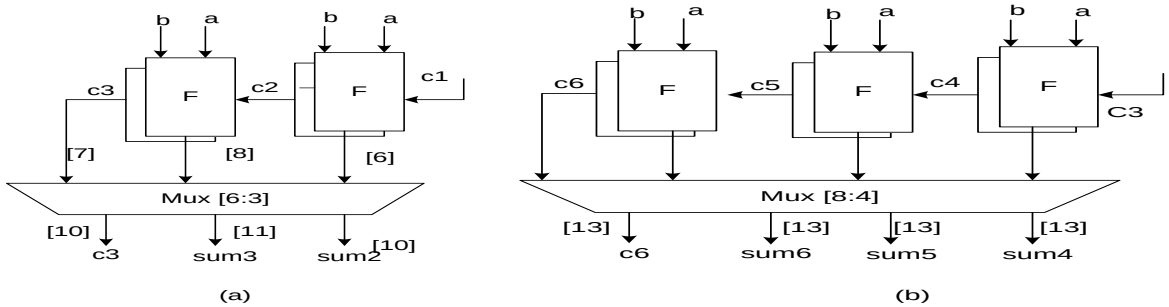


Fig.4 Regular 16 bit SQRT CSLA



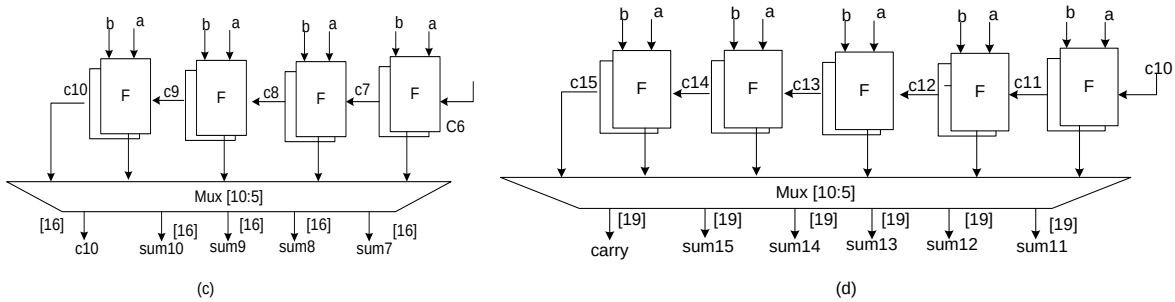


Fig.5 Delay and Area evaluation of regular SQRT CSLA : (a) group 2, (b) group 3, (c) group 4 and (d) group 5 where F is full adder.

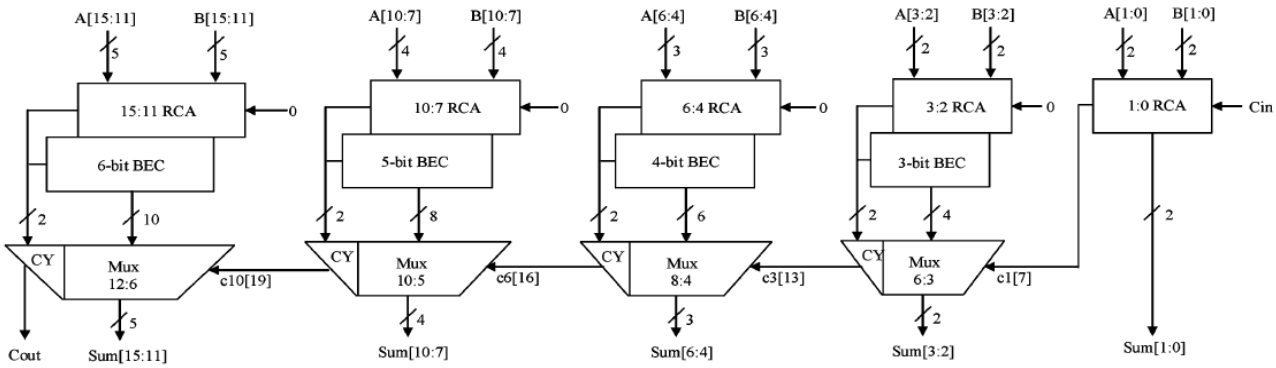


Fig.6 CSLA using BEC [4]

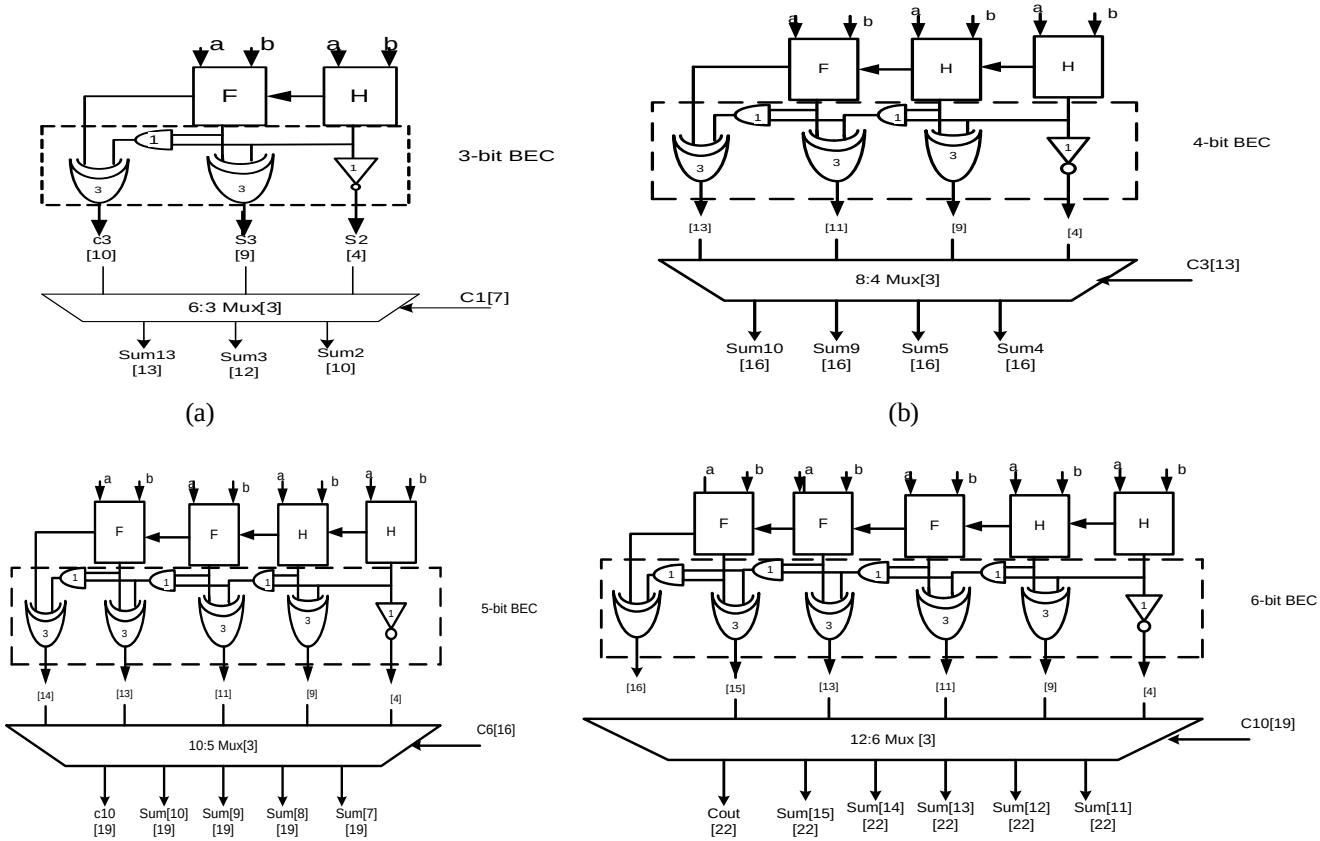


Fig.7 Delay and Area evaluation of modified SQRT CSLA : (a) group 2, (b) group 3, (c) group 4 and (d) group 5 where F is full adder. [4]

TABLE IV
Delay And Area Count Of Modified SQURT CSLA Groups

Group	Delay	Area
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

Table IV shows the delay and area count of the regular CSLA. There is a chance to reduce the area, power and delay in the CSLA structure.

VI . PROPOSED CSLA WITHOUT USING MUX

In this Proposed paper CSLA with cin=1 and multiplexer is replaced by the simple combinational circuit which consists of XOR and AND gates. By using this method area and power is reduced when compared to regular CSLA and modified CSAL (BEC). The modified 16-bit CSLA without using mux is shown in fig.8. The structure is again divided into five groups with different bit size RCA and Combinational.
Initially RCA structure is calculate for cin =0 the output of full adder is given to the combinational circuit and one of the input of that combinational circuit is previous stage carry then it will provide the proper output by using Xor and And gates structure. The group 2to 5 of the modified 16-bit CSLA is shown Fig.9.Comparing the group 2 to 5 of regular, modified BEC and WITHOUT MUX CSLA, it is clear that in this structure area is reduced.

TABLE V
Delay And Area Count Of Proposed SQURT CSLA Groups

Group	Delay	Area
Group2	12	36
Group3	18	55
Group4	23	74
Group5	29	87

Table V shows the delay and area count of the regular CSLA. Comparing Table III, IV and V its clear that the proposed design SQRT CSLA saves gate area when compared to regular SQRT CSLA and Modified BEC CSLA by slight increment in delay.

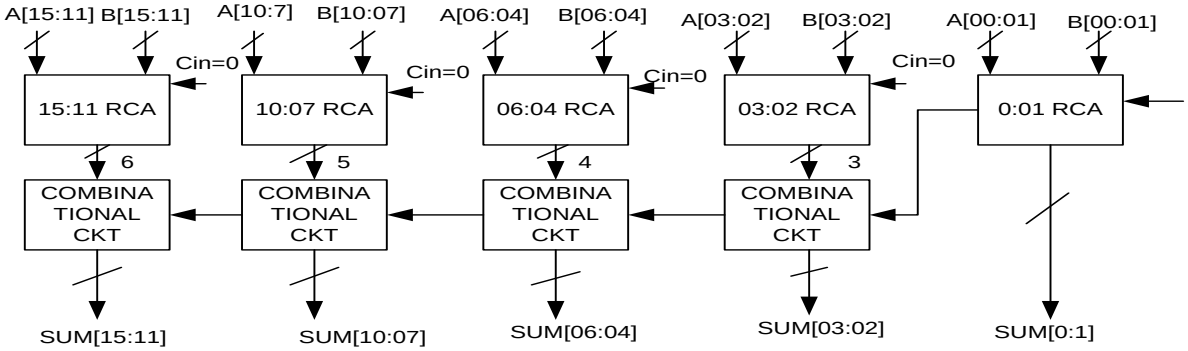
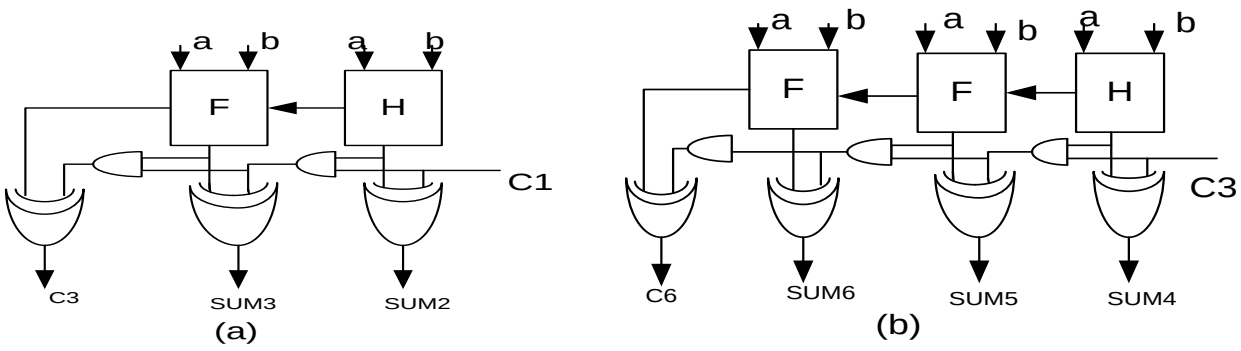


Fig .8 Proposed CSLA Without using multiplexer



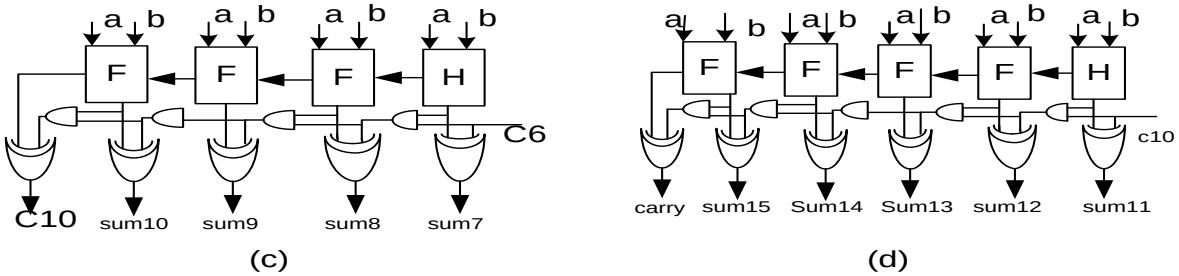


Fig.9 internal structure of Modified CSLA (Without using Multiplexer) (a) group 2, (b) group 3, (c) group 4 and (d) group 5 where F is full adder

VII. SIMMULATION RESULTS:

The design proposed in this paper has been developed using Verilog-HDL and synthesized in Synopsys RTL design compiler. The similar design followed for all regular, modified and Proposed SQRT CSLAs. Table VI to IX exhibits the simulation results of all the CSLA structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power. The percentage reduction in the cell area, total power, total delay, power-delay product and the area–delay product as function of the bit size are shown in below Table. Also plotted is the percentage area and power reduced in Fig.10. Fig10 (a) shows the percentage reduction in area. Fig10(b) shows the percentage reduction in power. It is clear that the area of the 8-, 16-, 32-, and 64-b proposed SQRT CSLA is reduced by 54.5%, 52.76%, 52.9%, and 51.56%, respectively when compared to regular SQRT CSLA. Power reduction of the proposed paper when compared to regular SQRT CSLA 8, 16, 32 and 64-b is 47.7%, 48.3%, 49.65% and 49.7%, respectively.

COMPARISON OF REGULAR AND MODIFIED SQRT CSLA WITH PROPOSED PAPER:

Table VI: 8-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)	Area delay product(10^ -12)
8 bit	Regular CSLA	2.195	955.937	15.241	33.45	2098.26
	BEC CSLA	3.336	628.906	14.229	47.46	2094.23
	Without Using MUX	3.337	434.843	7.956	26.55	1451.07

By observing the above table its clear when compared regular and modified circuit power and area is reduced and there is a slight increment in delay. But power delay and area delay product is reduced to almost half.

Table VII: 16-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)	Area delay product(10^ -12)
16 bit	Regular CSLA	4.848	2016.093	35.631	172.73	9774.00
	BEC CSLA	3.941	1362.031	33.458	131.793	5367.76
	Without Using MUX	6.201	952.343	18.413	114.14	5905.25

By observing the above table its clear when compared regular and modified circuit power and area is reduced and there is a slight increment in delay. But power delay and area delay product is reduced more.

Table VIII: 32-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)	Area delay product(10^ -12)
32bit	Regular CSLA	6.587	4161.562	77.499	510.48	27412.19
	BEC CSLA	6.729	2813.906	71.450	480.78	18934.73
	Without Using MUX	9.539	1958.593	39.0177	372.18	18682.99

By observing the above table its clear when compared regular and modified circuit power and area is reduced and there is a slight increment in delay. But power delay and area delay product is reduced more.

Table IX: 64-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)	Area delay product(10^ -12)
64 bit	Regular CSLA	11.169	8377.031	161.870	1807.92	93563.04
	BEC CSLA	11.181	5760.7812	147.69	1651.17	64411.28
	Without Using MUX	15.542	4057.3437	81.304	1263.40	63059.23

By observing the above table its clear when compared regular and modified circuit power and area is reduced and there is a slight increment in delay. But power delay and area delay product is reduced more.

Fig.11 shows the Simulation results of 64-bit CSLA without using multiplexer And Fig12 shows the power and delay calculation results by using synopsys of 64-bit CSLA without using multiplexer.

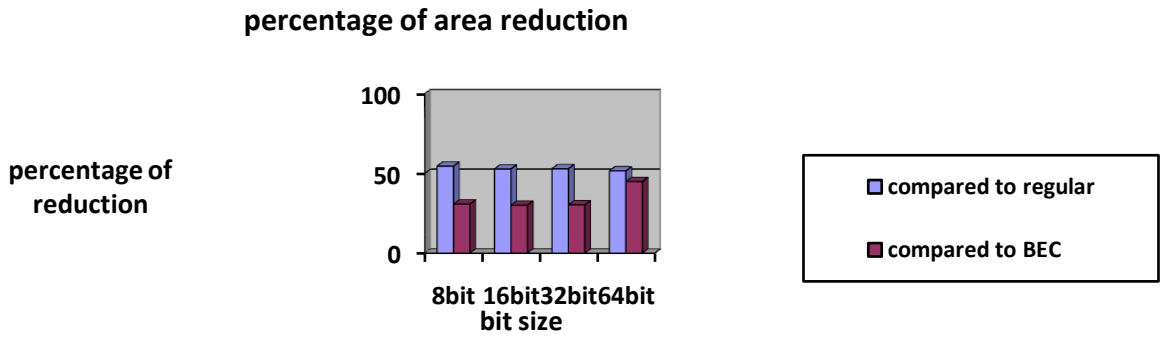


Fig .10(a) Percentage in Area reduction

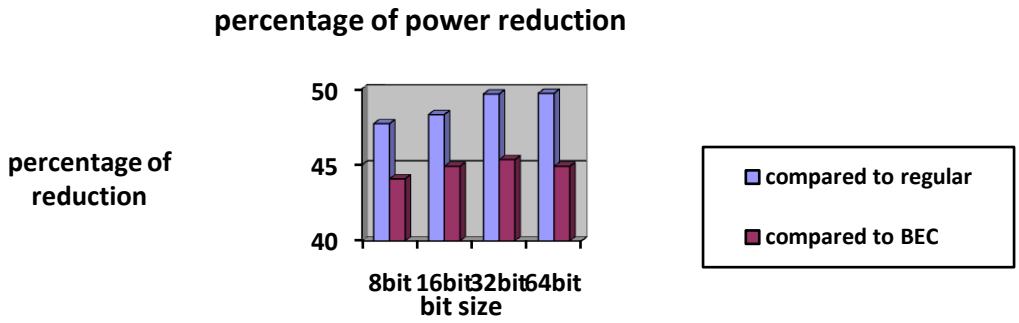


Fig .10(b) Percentage in Power reduction

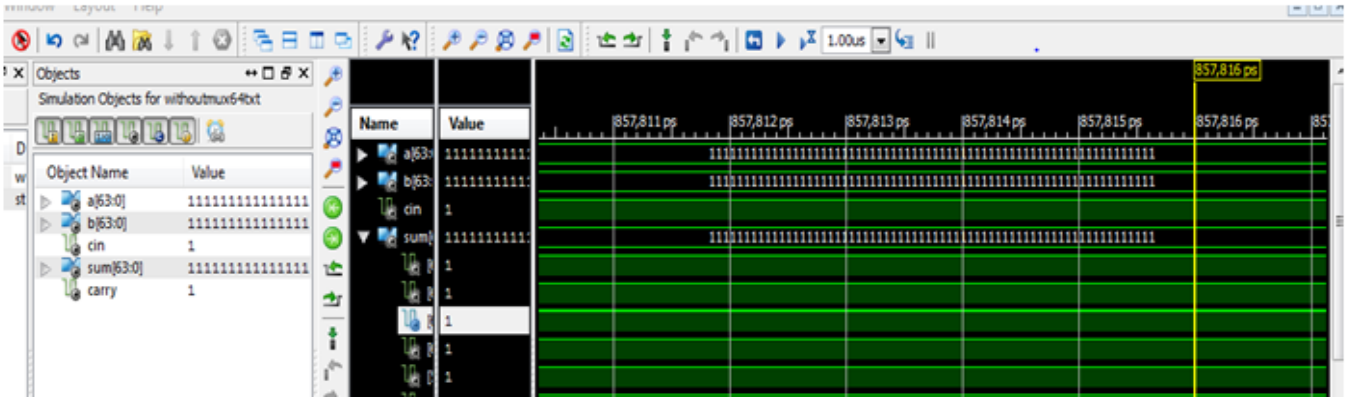


Fig.11 Simulation result of 64-bit CSA without using multiplexer

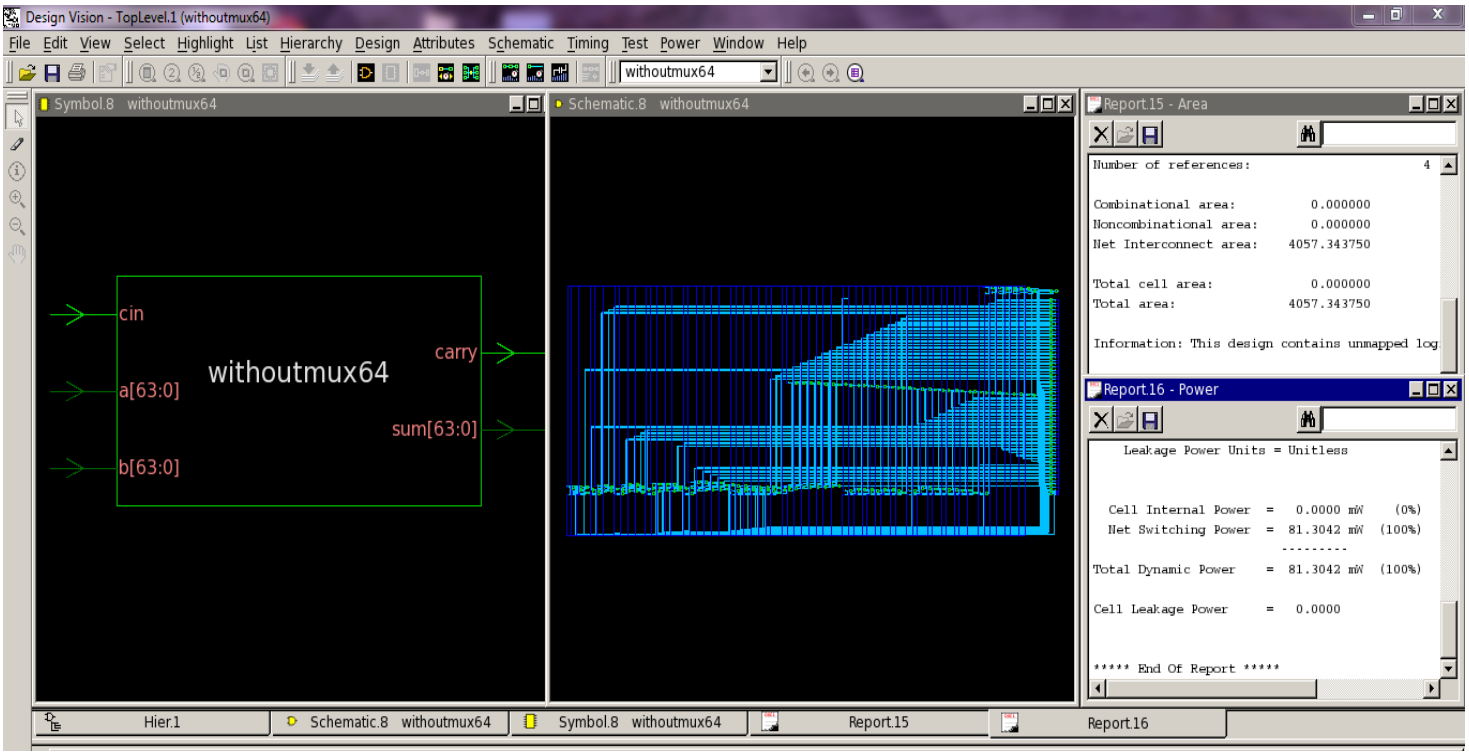


Fig.12 Power and Delay calculation of proposed circuit by using synopsys tool

VIII. CONCLUSION

A unique approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. This paper shows the design of carry select adder implemented by without using multiplexer and compared with regular and modified BEC CSLA. All these adders are implemented on Spartan XC3S500E FPGA device and the performance is compared. Power and Area is calculated by using synopsys RTL tool. This paper having better results when compared to regular and modified Carry Select Adder techniques.

References

[1] O. J. Bedrij, "Carry-select adder," *IRE Trans. Electron. Comput.*, pp.340–344, 1962.
[2] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," *Eur. J. Sci. Res.*, vol. 42, no. 1, p. 53–58, 2010.
[3] T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripple carry adder," *Electron. Lett.*, vol. 34, no. 22, pp. 2101–2103, Oct. 1998.
[4] B. Ramkumar and Harish M Kittur "Low-Power and Area-Efficient Carry Select Adder" *IEEE Trans. on very large scale integration systems* 2012.
[5] Feng Liu et.al "A Comparative Study of Parallel Prefix Adders in FPGA Implementation of EAC" *Proceedings of the 12thEuromicro conference on digital system design* 2009
[6] Matthew M. Ziegler and Mircea R. Stan "A Unified Design Space for Regular Parallel Prefix Adders" *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition 2004.*
[7] Konstantinos Vitoroulis and Asim J. Al-Khalili "*Performance of Parallel Prefix Adders implemented with FPGA technology"IEEE 2007.*
*[*14] He, Y. Chang, C. H. and Gu, J. (2005) 'An Area Efficient 64-Bit Square Root Carry-Select Adder For Low Power Applications', in Proc. IEEE Int. Symp. Circuits Syst., Vol.4, pp. 4082–4085
[9] Manoj Kumar, Sandeep K. Arya and SujataPandey,(December 2011) "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4,.
[10] Massimo Alioto and Gaetano Palumbo, (August 28-31, 2001,)"Optimized Design of Carry-Bypass Adders", ECCTD'01 - European Conference on Circuit Theory and Design, Espoo, Finland.
[11] Padma Devi, Ashima Girdher and Balwinder Singh, (June 2010)"Improved Carry Select Adder with Reduced Area and Low Power Consumption", International Journal of Computer Applications (0975 – 8887), Volume 3 -No.4,.
[12] Saiful Islam Md, Muhammad MahbuburRahman, Zerina begum and Mohd.Zulfiquar Hafiz, (2009)"Fault Tolerant Reversible Logic Synthesis: Carry Look-Ahead and Carry-Skip Adders", ACTEA 2009July 15-17, ZoukMosbeh, Lebanon.
[13] Akhilesh Tyagi, (1993) 'A Reduced-Area Scheme for Carry-Select Adders', IEEE Transactions on Computers, Vol.42, No.10, pp.1163-1170