International Journal of Innovative Research in Technology and Science

ISSN: 2321-1156 www.ijirts.org Volume 11 Issue 5, September 2023

Review of Design Challenges in Static Random-Access Memory (SRAM) Cell Circuits Based on Low Power Design (LPD)

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Abstract:- With the proliferation of portable devices in our daily lives, power optimisation has emerged as a primary challenge in modern VLSI technology. Various new gadgets and systems rely heavily on large-scale integration (VLSI) technology. Static random-access memory (SRAM) blocks occupy a significant portion of chip space and are the primary source of leakage power in many contemporary systems. Lowering the supply voltage of SRAM macros has been attempted to reduce power consumption; however, this often leads to increased power dissipation. Due to the growing process-related variations in read and write operation times, achieving stable SRAM cell operation at high power dissipation is increasingly challenging. In this research, we propose a method for scaling the supply voltage of SRAM macros, which effectively reduces overall power dissipation. We present 6T and 10T SRAM circuits that achieve significant power savings during read and write operations while maintaining reasonable performance and stability. Furthermore, the impact of process parameter variations on various design metrics, including read power, write power, leakage power, leakage current, and latency, becomes a critical concern as integration scales up in SRAM cell design. We introduce and compare the proposed 6T and 10T SRAM circuit cells, providing valuable insights into their performance characteristics.

Keywords: VLSI, Memory, SRAM, Low Power Design (LPD), Delay Write, Delay Read

Memory is utilised for storing data or information, and electronic memory devices typically employ two types of memory, volatile and non-volatile memory, depending on the specific application. These memory types significantly impact the speed and performance of electronic devices. In recent years, Static Random Access Memory (SRAM) has emerged as a pivotal breakthrough in research to enhance processing speed, reduce memory size, and lower power consumption. This demand has been driven by the increasing usage of advanced electronic devices such as laptops, IC memory cards, and more [1,2].

Cellular feedback mechanisms have been designed to enhance the performance of memory cells [3, 18], which are widely employed in low-leakage standby/on-off memory chips for mobile applications. Static memory functions as a semiconductor memory with a bistable latch circuit that stores and displays data memory on a per-bit basis. It's important to note that static memories are volatile, meaning the data they store is lost when not actively maintained within the memory cell, as depicted in Figure 1.

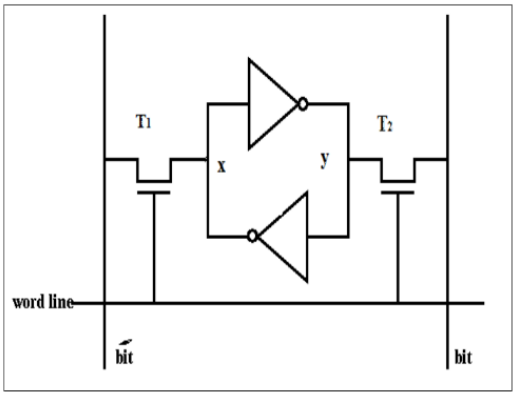

Figure 1: Memory Cell

SRAM, or Static Random Access Memory, represents semiconductor random access memory that uses latches or flip-flops to store data. The data stored in

SRAM persists indefinitely as long as continuous power is supplied. In contrast, the other type of random-access memory is DRAM (Dynamic Random Access Memory), which is also a semiconductor MOS memory but uses a capacitor and a transistor to store data. Both SRAM and DRAM are volatile. Despite its higher cost and lower packing density than DRAM, SRAM remains popular due to its exceptional speed. Data can be read from SRAM cells significantly faster than DRAM.

Additionally, SRAM does not require periodic refreshing like DRAM. As a result, SRAM is the preferred choice for designers in applications where high-speed performance is imperative and the cost of individual cells is tolerable, as is often the case in cache memory design. In the present era, where portable battery-powered devices have become ubiquitous, power dissipation and chip size have become major concerns. This has fuelled the demand for smaller, low-power consumption devices. With each passing day, the scale of integration continues to grow to accommodate smaller form factors and higher chip densities. However, this scaling technology introduces instability in the operation of SRAM cells. Conventional SRAM cells encounter various challenges in smaller technologies, such as leakage current and stability issues. To address the need for reliable designs in smaller technologies, various SRAM cell architectures have been developed. Given the trade-offs inherent in different SRAM cell parameters, optimising all aspects within a single design is not feasible.

Consequently, various SRAM cell designs have been developed to cater to diverse application requirements, focusing on optimising one or more specific parameters. This article delves into various SRAM cell designs, each composed of several transistors, highlighting their respective improvements and discussing the advantages and disadvantages of these distinct SRAM cell architectures. Traditional 6T SRAM Cell vs. Standard 6T SRAM Cells: In the standard 6T SRAM cell, there are two cross-coupled weak inverters used to store the state, along with some NMOS transistors that function as enable signals. These signals allow us to select which SRAM cell to read from or write to. The cross-coupled inverters serve as memory storage, while the NMOS transistors facilitate read and write operations on specific cells. This is how the two cross-coupled inverters function as memory elements.

When the input of the first inverter is logic 1, its output becomes logic 0, which in turn serves as the input for the second inverter. The output of the second inverter becomes 1, effectively closing the loop. This configuration operates with the word line transistors held at 0, isolating the cell from other cells. This design has an added advantage: the inverters ensure that the signal level does not degrade, eliminating the need for periodic data refresh, which is necessary in DRAM.

To read from or write data to the cell, we activate the cell by setting the word line (WL) to 1. This is accomplished by connecting a small line to the inverter. During a read operation, the bit line acts as the output, whereas during a write operation, it serves as the input. The latch immediately supports the GND and VDD voltages. The basic 6T SRAM cell is depicted in Figure 2. There are three operational states for SRAM cells: Maintenance Mode: In standby mode or maintenance mode (i.e., WL = 0), the access transistors M10 and M6 are blocked, breaking the connection with the bit line. -The data remains unchanged as long as the SRAM remains in this mode (provided the power supply remains connected). In this mode, only a leakage current flows. Write Operation: To perform a write operation on the SRAM cell, we need to "enable" it by raising the word line (WL). During write operations, we control the bit lines, which are considered input lines. The data we wish to write is transferred to bl, while BL_inv receives the complementary value. For instance, to write a logical '0' in the SRAM cell, we drive BL to 0 and BL_inv to 1. The WL signal determines SRAM cell selection. Data transmission occurs through transistors M10 and

M6. We complete the write operation when transistors M7 and M9 are open while M6 and M8 are closed. The SRAM cell will retain this value until overwritten by another write operation.

Read Operation: In a read operation, we also need to activate the WL. It is expected that the SRAM cell already contains a value before reading. When we "turn on" the cell, transistors M10 and M6 open, connecting bl and bl_inv in series. Preloaded rows are used to determine the values stored in memory as an SRAM cell holds the value 1. M8 and M11 are open in this case, while M9 and M7 remain closed. To read this data, we preload bl and bl_inv with high values and activate WL. Since M8 is open, activating WL has no effect on bl. However, for bl_inv, there will be a discharge in the circuit and current flow. Both bl and bl_inv are connected to a sense amplifier, which acts as a comparator and allows us to check the operation.

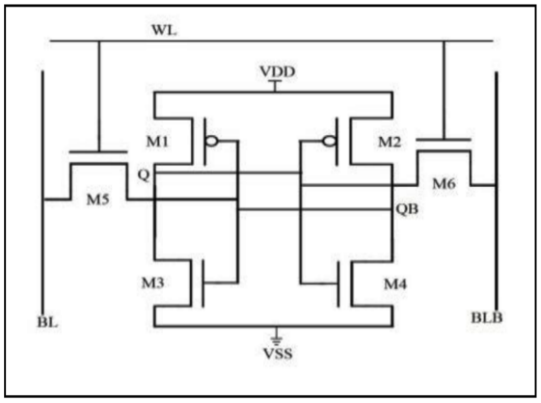

Figure 2: 6T SRAM Cell

II. Literature Survey

In the field of integrated circuits (IC), it is essential to address various challenges related to leakage current, gate leakage, and device variations resulting from CMOS scaling. Among the components of an IC, the Static Random Access Memory (SRAM) cell plays a crucial role. Researchers have explored innovative approaches to mitigate leakage issues, particularly in FinFET-based SRAM cells. One notable study by Safaryan et al. [8] focused on FinFET bit cells, where leakage has become a significant concern. They proposed an 8T SRAM cell design employing diode-connected NMOS/PMOS transistors to reduce leakage current effectively. Multiple techniques were employed to achieve this reduction, resulting in a substantial decrease in leakage power compared to the traditional 6T SRAM bitcell. The proposed 8T SRAM bitcell exhibited a remarkable threefold reduction in leakage power, an approximately 18% increase in read and write access times, and a 10% reduction in overall power consumption. These innovations were implemented using Synopsys Armenia Educational Department's SAED 14 nm technology. Carlson et al. [9] introduced a 5T SRAM cell design (Figure 3), which aimed to reduce area and power consumption compared to the conventional 6T SRAM cell. While this design offered advantages in terms of size and power, it faced challenges related to write '1' operations, relying on specific cell sizing strategies to ensure correct write operations. R. E. Aly et al. [10] introduced a 7T SRAM cell (Figure 4) with an additional NMOS transistor, N5, compared to the conventional 6T SRAM cell. The unique feature of this design was the disconnection of the feedback connection between two inverter pairs during the write operation, where N5 played a critical role. This design resulted in improved cell operation and lower write power dissipation, albeit at the expense of a 12.25% larger cell area.

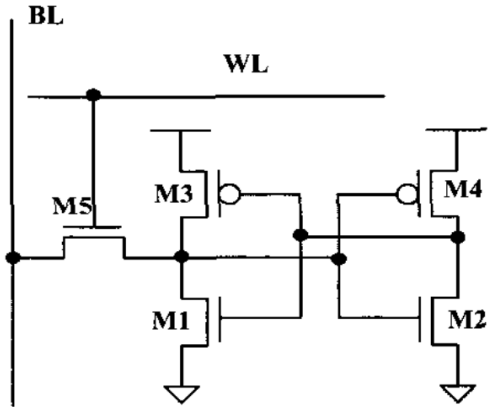

Figure 3: 5T SRAM Cell Schematic

V. K. Tomar et al. [11] analysed various SRAM cell topologies using 90nm technology and Cadence Virtuoso tools. They determined parameters such as read power, write power dissipation, read delay, write delay, write static noise margin (WSNM), and read static noise margin (RSNM) for these topologies. Notably, the 7T SRAM cell exhibited minimal read power, while the 8T SRAM cell demonstrated a

substantial 44.15% reduction in write power compared to the traditional 6T SRAM cell. Additionally, the 9T SRAM cell exhibited the shortest write delay. However, the highest RSNM was observed in the conventional 6T SRAM cell, while the 8T SRAM cell offered double the WSNM compared to the 6T SRAM cell. L. Chang et al. [12] presented the circuit diagram of an 8T SRAM cell (Figure 5) designed to enhance stability and allow for continued scaling. This cell featured separate read and write word lines and supported dual-port operation with separate read and write bit lines. The 8T SRAM cell provided advantages in terms of stability, higher static noise margin (SNM), and lower power consumption, but it consumed 30% more chip area than the conventional 6T SRAM cell.

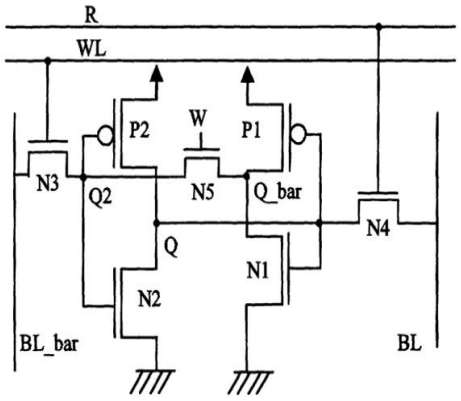

Figure4: Schematic of 7T SRAM Cell [5]

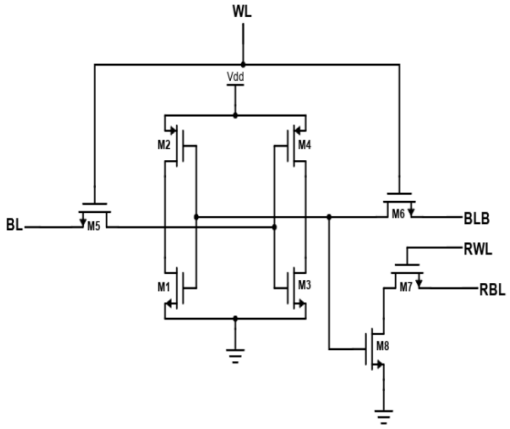

Figure 5. schematic of 8T SRAM cell

Z. Liu et al. [13] introduced a 9T SRAM cell (Figure 6) aimed at improving stability and reducing power consumption. This cell consisted of upper and lower sub-circuits responsible for data storage, bit line access, and read access. Notably, it achieved a 7.7% reduction in leakage power and better read stability than the traditional 6T SRAM cell. However, it occupied 37.8% more area due to three stacked transistors in the read circuit, which also increased the read access time. N. Arora et al. [14] addressed the growing demand for memory in the modern era, where SRAM operating voltage reductions had led to stability issues and increased process variation with scaling. They proposed a 10T SRAM cell design based on a gated-ground nMOS transistor technique to reduce total leakage power consumption while maintaining performance. Simulation results across various process nodes (90nm, 45nm, and 32nm) demonstrated the effectiveness of this technique in power reduction.

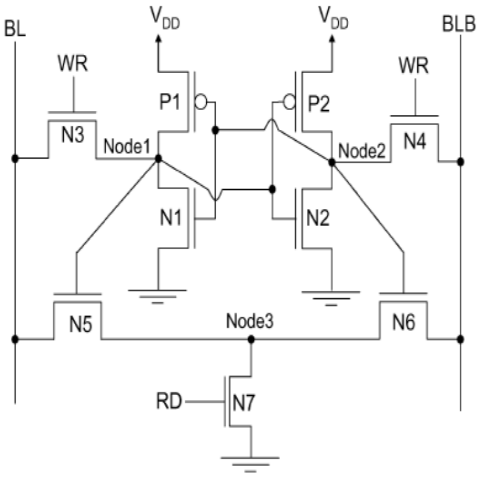

Figure 6. schematic of 9T SRAM Cell

III. Expect Outcome

This article introduces high-power consumption 6T and 10T SRAM differential cells. In the field of VLSI, where high power dissipation of SRAM cells is a concern, the proposed circuit design of the SRAM cell aims to reduce power dissipation. The proposed circuit design for the SRAM cell is also known as a power-saving device. To achieve improved and low power dissipation in all cases, the goal is to minimize power dissipation, establish benchmarks, and achieve the best possible efficiency.

IV.Conclusion

This article introduces high-power consumption 6T and 10T SRAM differential cells within the VLSI domain. These SRAM cells are known for their high power dissipation. We have explored various types of SRAM cells, all of which exhibit unique characteristics.

It is evident that in SRAM cell design, there exists a trade-off among different cell parameters, and this balance must be carefully considered during the design process. When compared to existing 6T and 10T SRAM cells, data storage in these cells can be complex due to their high power dissipation, resulting in a demand for substantial power and reduced speed. Our proposed technique addresses this limitation, providing higher speed with increased latency. Existing 6T and 10T SRAM cell design methodologies have been employed in constructing these SRAM cells. SRAM plays a pivotal role in integrated circuits, finding applications in high-speed processors and various portable devices. It is imperative that SRAM cells meet stringent requirements such as low power dissipation, minimal leakage current, and operation in the sub-threshold region. We have investigated various methodologies utilized in different SRAM cells with a focus on designing low-power SRAM solutions. Our proposed circuit design for SRAM cells is recognized as an energy-efficient solution. Our ultimate goal is to achieve improved and low power dissipation under all circumstances, ensuring reliability in SRAM operation..

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