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Design, Implementation, and Performance Analysis of an SRAM Cell for Low-Power Consumption Applications

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Abstract: SRAM cells play a crucial role in memory designs and find applications in various systems on chips (SoCs). Considering the continuous technological advancements and the need for energy-efficient operation, power dissipation and low power consumption are critical concerns in SRAM cell design. This study proposes a circuit design based on the switching concept to achieve power savings in SRAM cells for low-power consumption applications. The primary objective of the proposed circuit design is to minimise power usage in different devices. As memory cell operation with low voltage consumption gains prominence in low-energy computing, the design of SRAM cells becomes a significant area of research. With its high storage density and quick access time, SRAM has become a vital component in VLSI chips used in notebooks, laptops, IC memory cards, and handheld communication devices. This work explores the write, read, dynamic, and static power consumption and voltage and temperature characteristics of an SRAM circuit for smart applications. Power consumption analysis is a critical criterion in memory design, impacting reading and writing activities. The implemented 6T, 8T, and 10T SRAM cells, along with the proposed circuit design, demonstrate superior efficiency in power usage compared to existing SRAM topologies. By considering different parameters such as write power, read power, and idle time power, the proposed circuit design outperforms the traditional SRAM (6T, 8T, and 10T) circuits. As specifications change with scaling approaches, ensuring SRAM stability becomes crucial for successful low-voltage SRAM design. Simulation results indicate that the proposed design enables faster read operations and optimises the total power delay product. While addressing the read disruption problem encountered in conventional SRAM cells, our primary goal is to reduce power consumption and improve read and write delay performance, as these factors significantly impact memory cell performance.

Keywords: Very Large-Scale Integrated Circuits, Device Circuit, SRAM, Delay Write, Delay Read, power delay product optimisation, Low Power Design, Energy Efficient Device.

I. Introduction

Static random-access memory (SRAM) is a type of semiconductor memory that stores each bit using bistable latching circuitry. Unlike dynamic RAM (DRAM), which requires regular refreshing, SRAM can retain data without the need for refreshing. However, SRAM is still considered volatile because data is lost when the memory is powered off.

Scaling bulk CMOS to 32nm gate lengths faces several challenges, including short channel effects, sub-threshold leakage, gate-dielectric leakage, and device-to-device variations. These factors pose significant barriers to achieving further scaling. Ultra-short channel devices, such as 6T SRAM cells and their modifications, experience an abrupt increase in threshold voltage (Vt) oscillation due to overall and general process variations. Consequently, these devices cannot be operated at advanced supply voltage scaling without functional and parametric failure, leading to yield loss.

The design of a standard 6T SRAM cell encounters various issues related to write delay. While the Low power 6T SRAM cell design successfully reduces write power and access delay, it does not address the stability issue [1].

Memory cells serve as the fundamental building blocks of computer memory. A memory cell is an

electronic circuit that stores one bit of binary information. It can be set to store logic 1 (high voltage level) or reset to store logic 0 (low voltage level). The stored value remains retained until it is changed.

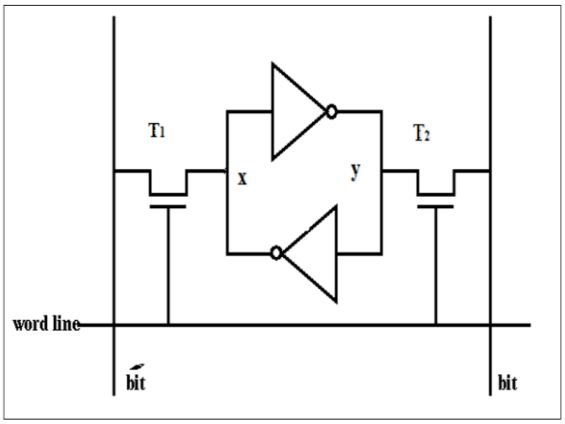

Figure 1: represents a memory cell

The main objective of this research is to develop a modified SRAM cell with low power consumption. This modification enables faster execution and simulation of transistor applications in both the analogue and digital domains. FinFET (Fin Field Effect Transistor) technology is considered a promising option for future nanoelectronics due to its compact nature, high performance, low manufacturing costs, and low power consumption. FinFETs can potentially replace bulk CMOS transistors. With their low leakage current and standby power, FinFETs are well-suited for designing memory subsystems.

The researchers employed the VLSI integration procedure (Very Large-Scale Integration) in their study. VLSI refers to the process of integrating millions of transistors onto a single chip, resulting in an Integrated Circuit (IC). Advancements in VLSI have led to the emergence of innovative technologies that enhance circuit speed while minimising design constraints [2].

1.1 SRAM Cells and Their Operation

The foundation of any static memory system is the SRAM cell. Figure 2 illustrates a conventional CMOS 6-transistor (6T) static memory cell. This circuit consists of two cross-coupled inverters and two access transistors, M5 and M6 [3].

Standby Mode: In standby mode (word line=0), the pass transistors M5 and M6, which connect the 6T cell to the bit lines, are turned off. Consequently, the cell is inaccessible. As long as N1 and N2 are connected to the power supply, the two cross-coupled inverters will continue to provide feedback to each other, storing the data in the latch [4].

Read Mode: The word line (WL) and bit lines (BL) are held at VDD during a read operation. The feedback from the cross-coupled inverters is initially disconnected. Then, by sweeping Q (the input of the inverter) from 0 to VDD and measuring QB (the output of the inverter), the voltage of the inverter formed by half of the SRAM cell is determined [5].

Write Mode: In a write operation, VDD is applied to the word line, and the value to be written into the memory cell is driven onto the bit lines. Figure 1 demonstrates calculating the write static noise margin (SNM). Once again, the feedback from the cross-coupled inverters is broken, and the inverter voltage is measured. However, in this case, the voltages of the two halves of the SRAM cell are no longer the same (because one of the bit lines is driven to 0V and the other to VDD) [6].

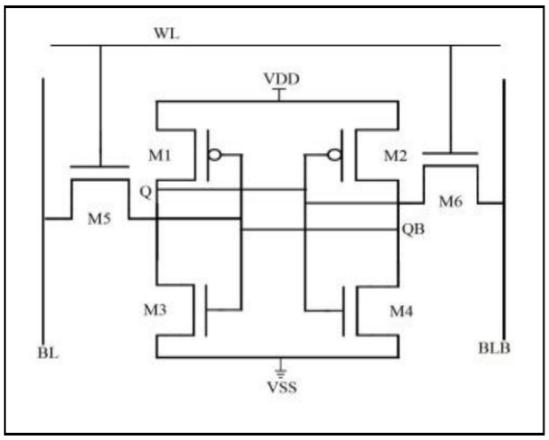

Figure 2: shows the schematic diagram of a 6T SRAM cell.

II. Literature Survey

K. Takeda et al. [7] investigated the limitations of conventional 6T SRAM cells. In the conventional design, the read operation is performed by activating the word line and accessing the latch through the access transistors. However, this approach can lead to data disturbance and corruption due to static noise. Additionally, the

read operation in the 6T cell is relatively slow because it takes time to activate the access transistors and access the latch. Slow read operations in SRAM increase leakage power during idle periods, negatively impacting cell performance and making it unsuitable for practical applications. Mishra S et al. [8] proposed a seven-transistor (7T) SRAM cell design. This design consists of two CMOS inverters that are internally latched using an additional NMOS transistor connected to the read line. The cell also includes two NMOS access transistors connected individually to the bit line bar and bit line. In the 7T SRAM cell depicted in Figure 2, the M5 access transistor is connected to the word line (WL) and is responsible for the write operation, while the M6 transistor is connected to the read line (R). During read and write operations, the bit line is the input/output node, carrying information to the sense amplifier.

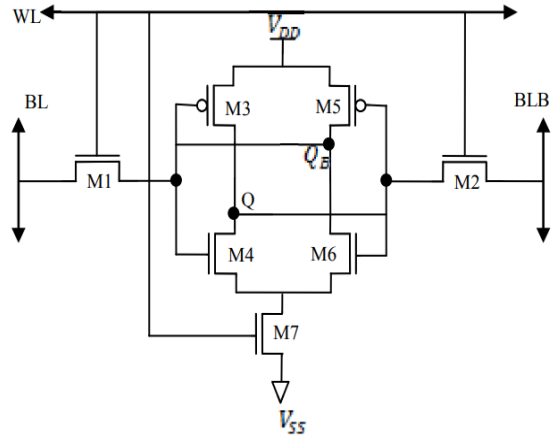

Figure 3: depicts the schematic diagram of a 7T SRAM cell.

D. Mittal et al. [9] proposed an 8T SRAM cell design to overcome some 6T SRAM circuit limitations. The 8T SRAM cell includes a separate read port, as depicted in Figure 4. By introducing this additional read port, the design aims to enhance the read operation and improve the overall performance of the SRAM cell. The figure shows that C. Yu et al. [10] proposed a 9T SRAM cell architecture incorporating the 6T write cell and three additional transistors for the read circuit. The write operation in this 9T SRAM cell is similar to that of the 6T circuit, where the write word line (WWL) is charged to activate the access transistors, and data is applied to the bit lines. The stored data is stored in the nodes Q and Qb. The WWL is set to zero voltage during the read operation, and the read bit-line (RBL) is pre-charged. When the read word line (RWL) is charged, the RBL will discharge through M7 and M8 if a '0' is stored in Q (corresponding to a '1' in Qb).

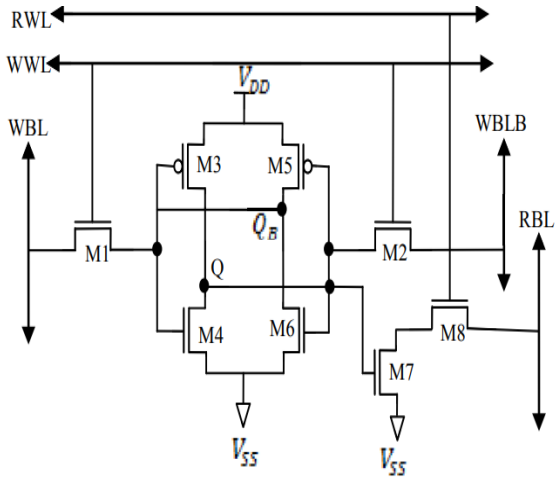

Figure 4: illustrates the schematic diagram of an 8T SRAM cell.

Conversely, if a logic '1' is stored in Q (corresponding to a '0' in Qb), the RBL will not discharge and remain at a high logic level. It is important to note that although the write signal can be applied to this circuit during the read function, the RBL needs to be recharged before the next read operation. Including the additional transistors in the read circuit of the 9T SRAM cell improves the read static noise margin (RSNM) compared to the 6T SRAM cell. The storage nodes are isolated from the read path, contributing to this improved noise margin.

In work by Singh S et al. [11], they propose a fully differential low-power 10T SRAM bit cell, as depicted in Fig. 2.3. The design strategy of this cell involves the series connection of a tail transistor. The gate electrode of this transistor is controlled by the output of an XOR gate, with inputs tapped from the write word line (WWL) and read word line (RWL) control signals generated by the WWL and RWL drivers. It's worth mentioning that all the cells in a row share the XOR gate and the tail transistor. The tail transistor must be appropriately sized to handle the sinking currents from all the cells in the row. This read buffer is crucial as, without it, a cell with small drivers and

a series-connected tail transistor would exhibit an unacceptably low read static noise margin (RSNM), resulting in read instability. By incorporating this fully differential design and the appropriate read buffer, the proposed 10T SRAM cell aims to overcome the read instability issues associated with using small drivers and a series-connected tail transistor.

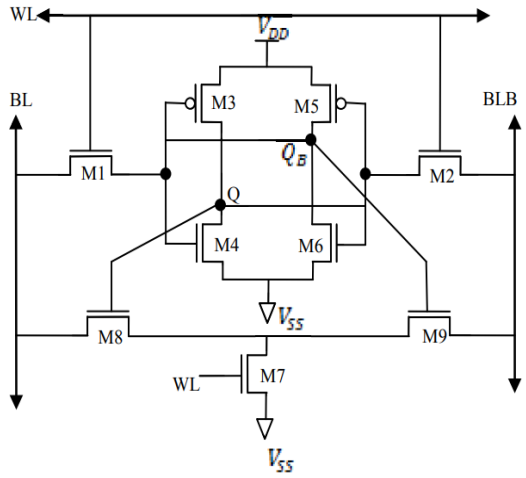

Figure 5: displays the schematic diagram of a 9T SRAM cell.

III Simulation Software

Microwind Tools is a simulation software for designing and modelling circuits at the layout level. It provides a range of features and capabilities for chip designers to plan and implement their innovative ideas. Microwind combines front-end and back-end chip designs, streamlining the planning process and reducing complexity. The software integrates various functionalities such as message execution, circuit replication, semiconductor-level mining, and verification, offering a comprehensive platform for learning and developing skills required in the integrated circuit industry. Microwind enables designers to reconstruct and design integrated circuits at the current level. It offers schematic passes, design-based test systems, SPICE extraction in schematic, Verilog extract, format accumulation, signal mix format, signal extraction, netlist extraction, BSIM4 teaching exercises, and closed connections. The software includes a library of standard components and facilitates easy viewing and replicating ICs. It also provides a coverage checker for circuit analysis and simulation. With Microwind, users can perform circuit simulations using voltage and flux bending methods. The software supports full editing capabilities, multiple views including MOS characteristics, 2D cross-section, 3D process viewer, and an analogue simulator. It offers a user-friendly interface and features an online testing mechanism. Microwind is a comprehensive circuit design and simulation tool at the layout level.

IV. Results Analysis

The result analysis based on 6T, 8T, 10T, and PSCBLCA SRAM cells evaluated various parameters, including compression read delay, write delay, and idle mode power consumption.

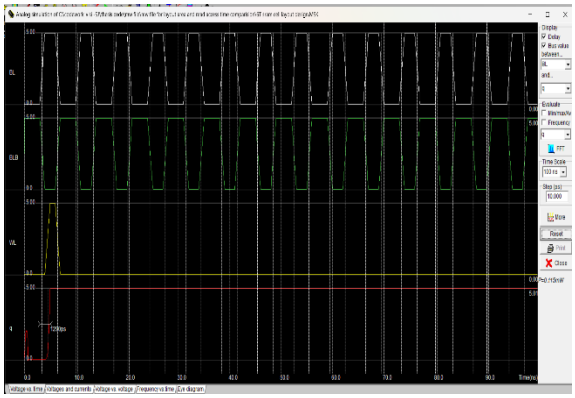

Figure 6: Micro Wind depicts the layout of an existing circuit showing the read operation time of a 6T SRAM cell.

(a) Read Delay Time-based Power Use Analysis:

The power consumption during the read delay operation was analysed for 6T SRAM, 8T SRAM, 10T SRAM, and PSCBLCA. A comparison was made between the traditional circuits (6T SRAM, 8T SRAM, 10T SRAM) and the proposed circuit (PSCBLCA) regarding power usage during the read delay for different input voltages. The impact of the supply voltage was a significant limitation that affected the device's reliability in playback mode and had overall implications on its suitability.

(i) RD-6T:

In the analysis of RD-6T SRAM, the voltage was varied from 0.4V to 1V. The power consumption for all activities was measured relative to the standard voltage. The RD-6T SRAM refers to a single-piece SRAM cell, as shown in Figure 6.

(ii)RD-8T:

In the analysis of RD-8T SRAM, the voltage was varied from 0.4V to 1V. The power consumption for all activities was measured relative to the standard voltage. The RD-8T SRAM refers to a single-piece SRAM cell, as shown in Figure 7.

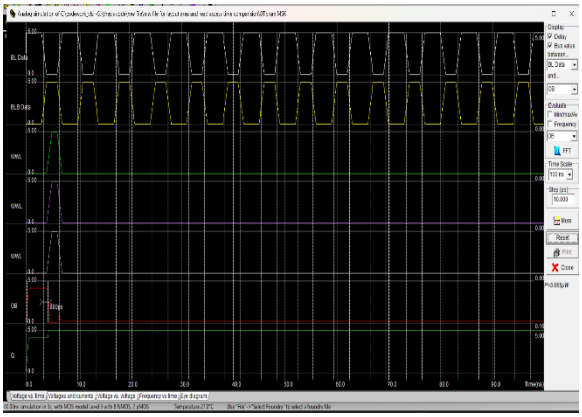

Figure 7: Micro Wind presents the layout of an existing circuit showing the read operation time of an 8T SRAM cell.

(iii) RD-10T

In this analysis of the existing circuit for the read operation time of 10T SRAM, the voltage was varied from 0.4V to 1V. The power consumption for all activities was measured relative to the standard voltage. The existing circuit for the read operation time of 10T SRAM refers to a single-piece SRAM cell, as shown in Figure 8.

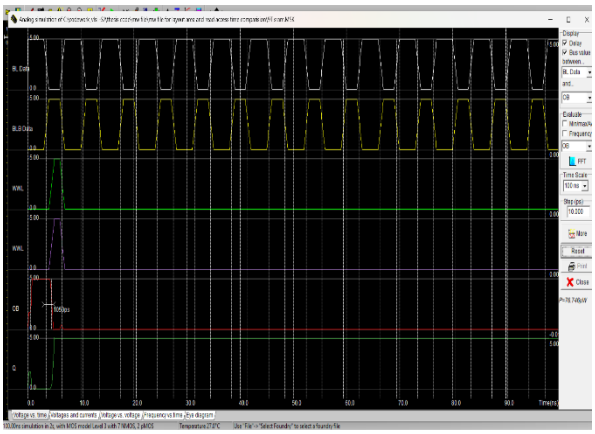

Figure 8: represents the layout in Micro wind, demonstrating the existing circuit for a 10T SRAM and showing its read operation time.

(iv) RD- PSCBLCA

In this analysis of the proposed circuit, the read operation time of PSCBLCA is evaluated by shifting the voltage from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 9 depicts the single-piece SRAM cell used in the read operation of RD-PSCBLCA.

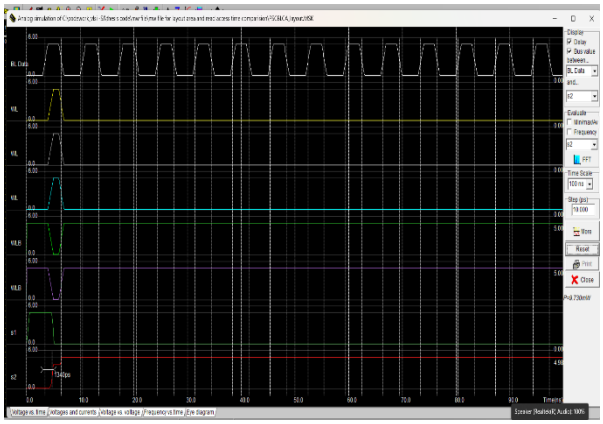

Figure 9: layout in Micro wind show proposed circuit read operation time PSCBLCA.

Table 1 presents the power consumption versus supply voltage comparison of existing 6T, 8T, 10T, and PSCBLCA circuit's read operation time for SRAM Cells.

SRAM Cells	Time Scale (in ns)	Power Consumption (uw)
6T	100	0.115
8T	100	5.666
10T	100	76.746
PSCBLCA -RD	100	9.73

(v) Overview of Power Consumption Analysis Based on Read Delay Time

The power consumption of the current read delay operation time is analysed in 6T SRAM, 8T SRAM, 10T SRAM, and PSCBLCA. A comparison is made between the power usage of the old circuits (6T SRAM, 8T SRAM, 10T SRAM) and the proposed circuit (PSCBLCA) in the analysis of power consumption during read delay for various input voltages. Table 1 demonstrates that the power utilisation of the proposed PSCBLCA-RD Cell configuration increases with the increasing supply voltage from 0.5V to 1V. It is evident from Table 5.1 that the PSCBLCA-RD memory configuration consumes less power than the existing 8T and 10T memory designs. Figure 10 illustrates this comparison.

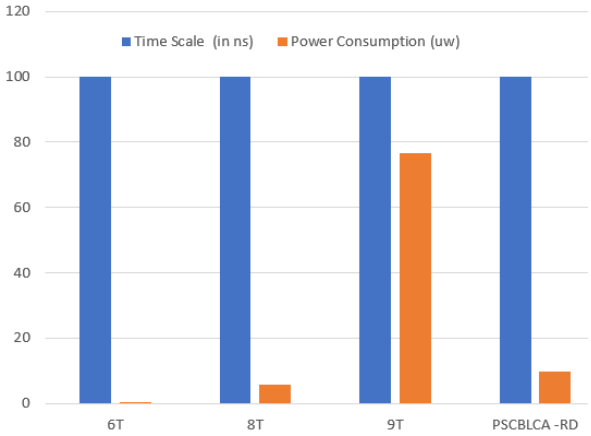

Figure 10: Power Consumption Analysis of Read Operation Time between 6T, 8T, 10T, and PSCBLCA.

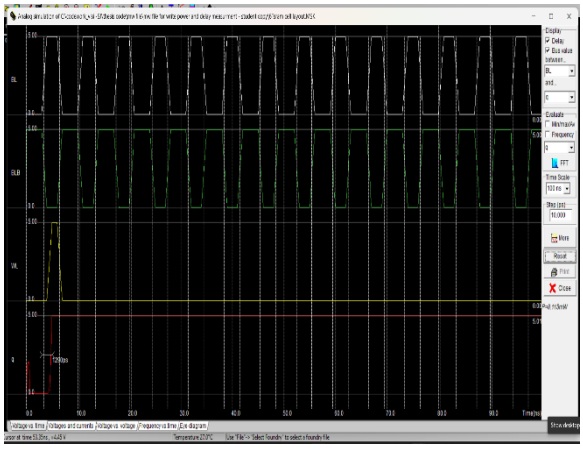

Figure 11: Layout in Micro wind illustrating the existing circuit for write operation time in 6T SRAM.

(b) Write Delay Time-based Power Use Analysis:
The power consumption of the current write delay operation time is analysed in 6T SRAM, 8T SRAM, 10T SRAM, and PSCBLCA. A comparison is made between the power usage of the old circuits (6T SRAM, 8T SRAM, 10T SRAM) and the proposed circuit (PSCBLCA) in the analysis of power consumption during write delay for different input voltages. The impact of supply voltage is a significant limitation that affects the stability and reliability of the phone in real mode. It is advisable to have a higher supply voltage for increased SRAM and cell strength.

(i) WD-6T

In this analysis of the write operation time in 6T SRAM, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 11 showcases the single-piece SRAM cell used in the write operation of the 6T SRAM.

(ii) 8TWD
In this analysis of the write operation time in 8T SRAM, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 12 showcases the single-piece SRAM cell used in the write operation of the 8T SRAM.

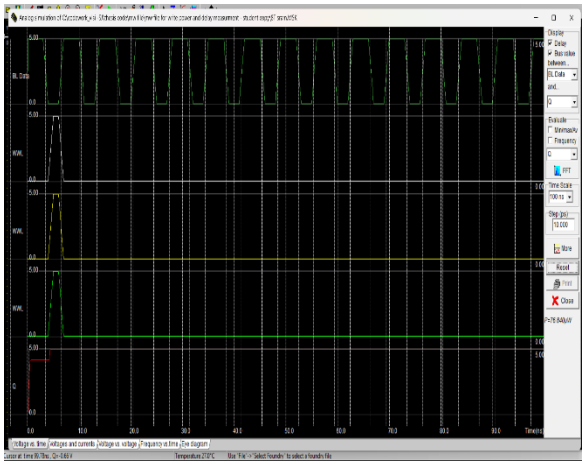

Figure 12: Layout in Micro wind illustrating the existing circuit for write operation time in 8T SRAM.

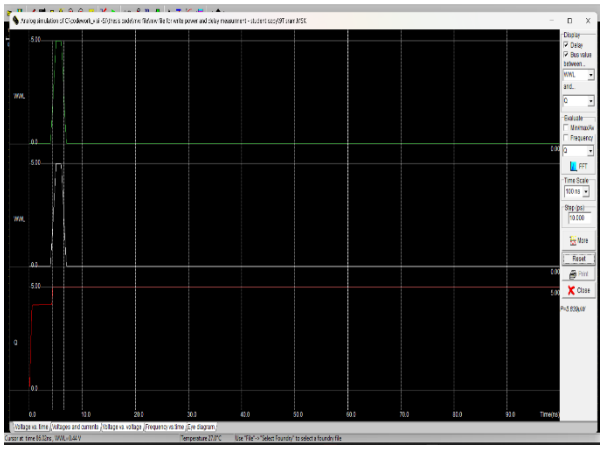

Figure 13: Layout in Micro wind illustrating the existing circuit for write operation time in 10T SRAM.

(iii) 10TWD

In this analysis of the write operation time in 10T SRAM, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 13 showcases the single-piece SRAM cell used in the write operation of the 10T SRAM.

(iv)WD- PSCBLCA

In this analysis of the write operation time in WD-PSCBLCA, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 14 showcases the single-piece SRAM cell used in the write operation of WD-PSCBLCA.

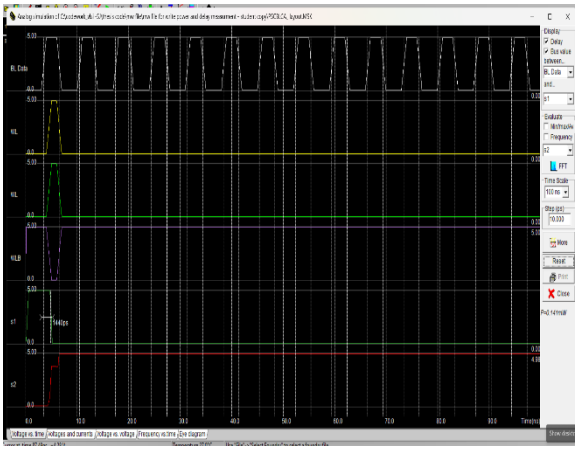

Figure 14: Layout in Micro wind illustrating the proposed circuit for write operation time in PSCBLCA.

(v) An Overview of Power Consumption Analysis Based on Write Delay Time.

The power consumption of the current write delay operation time is analysed in 6T SRAM, 8T SRAM, 10T SRAM, and PSCBLCA. A comparison is made between the power usage of the old circuits (6T SRAM, 8T SRAM, 10T SRAM) and the proposed circuit (PSCBLCA) in the analysis of power consumption during write delay for different input voltages. Table 2 shows that the power utilisation of the proposed PSCBLCA-WD Cell configuration increases with the increasing supply voltage from 0.5V to 1V. It is evident from Table 5.1 that the PSCBLCA-WD memory configuration consumes less power than the existing 8T and 10T memory designs. Figure 15 provides a visual representation of this comparison.

Table 2: Power Consumption vs Supply Voltage of Existing 6T, 8T, 10T, and PSCBLCA Circuits for Write Operation Time in SRAM Cells.

SRAM Cells	Time Scale (in ns)	Power Consumption (uw)
6T	100	0.115
8T	100	76.84
10T	100	5.839
PSCBLCA - WD	100	0.141

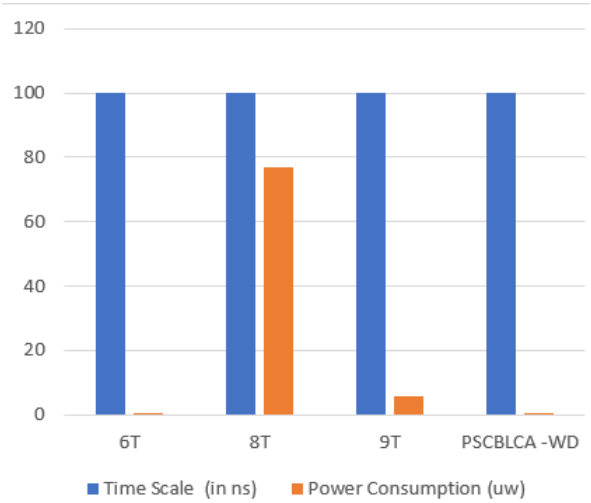

Figure 15: Power Consumption Analysis of Write Operation Time between 6T, 8T, 10T, and PSCBLCA.

c) Power Use Analysis:

The power consumption of the current idle mode operation time is analysed in 6T SRAM, 8T SRAM, 10T SRAM, and PSCBLCA. A comparison is made between the power usage of the old circuits (6T SRAM, 8T SRAM, 10T SRAM) and the proposed circuit (PSCBLCA) in analysing power consumption during idle mode for different input voltages. The impact of supply voltage is a significant limitation that affects the reliability of the phone in real mode. In the idle mode, the inventory voltage should be highest to increase SRAM performance and enhance cell strength.

(i) 6T

In this analysis of the idle mode time in 6T SRAM, the voltage varies from 0.4V to 1V. The power

consumption for all activities is measured relative to the standard voltage. Figure 16 showcases the single-piece SRAM cell used in the idle mode time of the 6T SRAM.

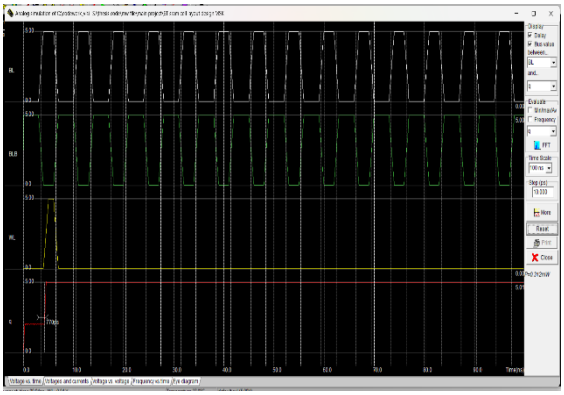

Figure 16: Layout in Micro wind illustrating the existing circuit for idle operation time in 6T SRAM.

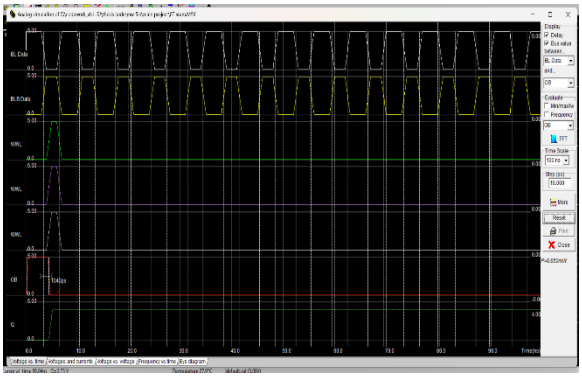

Figure 17: Layout in Micro wind illustrating the existing circuit for idle operation time in 8T SRAM.

(i) 8T:
In this analysis of the idle mode time in 8T SRAM, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 17 showcases the single-piece SRAM cell used in the idle mode time of the 8T SRAM.

(i) 10T
In this analysis of the idle mode time in 10T SRAM, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 18 showcases the single-piece SRAM cell used in the idle mode time of the 10T SRAM.

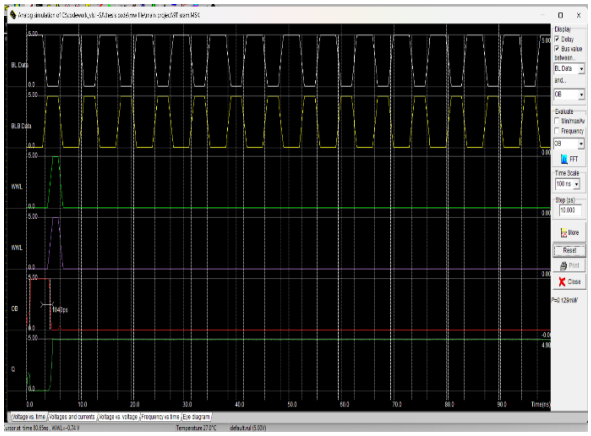

Figure 18: Layout in Micro wind illustrating the existing circuit for idle operation time in 10T SRAM.

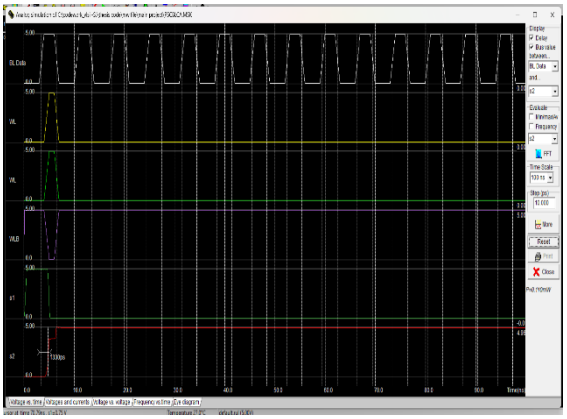

Figure 19: Layout in Micro wind illustrating the proposed circuit for idle operation time in PSCBLCA.

(iv) PSCBLCA:
In this analysis of the idle mode time in PSCBLCA, the voltage varies from 0.4V to 1V. The power consumption for all activities is measured relative to the standard voltage. Figure 19 showcases the single-piece SRAM cell used in the idle mode time of the PSCBLCA.

Table 3: Power Consumption vs Supply Voltage of Existing 6T, 8T, 10T, and PSCBLCA Circuits for Idle Operation Time in SRAM Cells.

SRAM Cells	Time Scale (in ns)	Power Consumption (uw)
6T	100	0.312
8T	100	6.65
10T	100	0.129

PSCBLCA	100	0.11

(v) An Overview of Power Consumption Analysis Based on Idle Mode Time.

The power consumption of the current idle mode time operation is analysed in 6T SRAM, 8T SRAM, 10T SRAM, and PSCBLCA. A comparison is made between the power usage of the old circuits (6T SRAM, 8T SRAM, 10T SRAM) and the proposed circuit (PSCBLCA) in the analysis of power consumption during idle mode time for different input voltages. Table 3 shows that the power utilisation of the proposed PSCBLCA-idle mode time Cell configuration increases with the increasing supply voltage from 0.5V to 1V. It is evident from Table 5.3 that the PSCBLCA memory configuration consumes less power than the existing 6T, 8T, and 10T memory designs. Figure 20 provides a visual representation of this comparison.

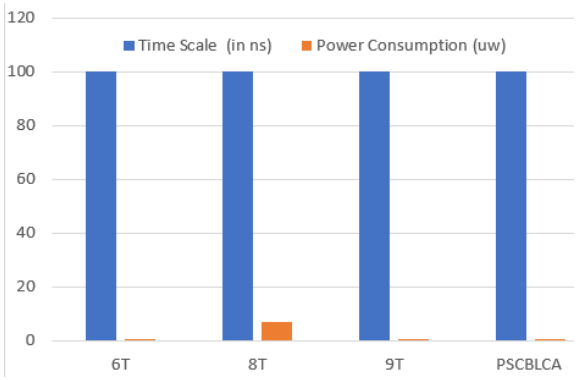

Figure 20: Power Consumption Analysis of Idle Operation Time between 6T, 8T, 10T, and PSCBLCA.

Conclusion

The design implementation and performance analysis of SRAM cells using low-power consumption applications, specifically the proposed switching concept based on PSCBLCA, have been presented. The simulation results demonstrate improvements in both the read and write power of conventional 6T, 8T, and 10T SRAM cells. Higher SRAM performance can be achieved by modifying the device parameters of the conventional SRAM cells without requiring any modification to the SRAM cell array design. The performance metrics of various SRAM cell topologies, including the conventional ones, have been compared, focusing on leakage currents, power, and reading behaviours. The results indicate that the proposed SRAM cell models exhibit significant reductions in leakage current and power dissipation compared to the conventional SRAM cells. However, it is important to address the challenges related to reading operation time, as increased leakage power and reduced read stability can lead to data corruption due to external noise. The proposed circuit design considers the limited use of supply voltage in electronic devices. As a result, power consumption reduction has become a crucial requirement in designing new architectures for integrated circuits. The development of the proposed circuit design for leakage reduction was implemented using the micro wind tool. Both delay and power consumption are critical factors in achieving optimal memory cell performance. In summary, the primary objectives of this work were to reduce power consumption, improve read delay performance, improve write delay performance, and enhance the overall memory cell performance by considering important factors such as power consumption and reliability.

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