International Journal of Innovative Research in Technology & Science

ISSN: 2321-1156 ***Volume V, Issue VI, November, 2017***

Enhancement Low Power Static Random Access Memory: A Review

Akanksha Kanday, M. Tech. Scholar, Department of EC, TIT, RGPV, Bhopal, India, akanksha02k@gmail.com;
Dr. Vibha Tiwari, Professor, Department of EC, TIT, RGPV, Bhopal, India, vibhatiwari19@gmail.com;

Abstract

Memories are the crucial a part of any digital system and no digital system may be completed without memories. Compact devices and embedded systems are emerging, therefore the low power consumption is extremely essential to the architectural system design .Optimization of the ability at the logical level is one amongst the foremost necessary task to reduce the ability. Performance in terms of speed and power dissipation is that the major areas of concern in today's memory technology. During this paper SRAM cells supported 6T and 8T configurations are compared on the idea of performance for browse and write operations. During this paper survey on completely different static random access memory is designed so as to high power, high performance circuit and therefore the intensive survey on options of various static random access memory (SRAM) designs was reported. During this paper survey a strong traditional SRAM is designed however our aim is to use change circuits to induce best throughput for SRAM are often achieved. Projected design is designed victimization change principles. Projected SRAM is tested on micro wind tool.

Keywords: - Memories, SRAM, Delay, stability, Power Consumption, 6T-SRAM.

I. INTRODUCTION

Low power SRAMs have become a vital part of the many VLSI chips. this is often especially true for microprocessors, wherever the on-chip cache sizes are growing with every generation to bridge the increasing divergence within the speeds of the processor and also the main memory .Due to the exaggerated integration and in operation speeds, power dissipation has become a very important thought each similarly as because of the explosive growth of battery operated appliances. Planning electronic systems victimization digital techniques has become a well-accepted commonplace with electronic design community. The preciseness and speed of any machine block in digital design may be increased by simply widening the information bus and creating computational blocks compatible with widened data bus. Therefore a complex digital electronic system handles wide data buses, addresses large memory space and embeds the logical and procedure blocks with acceptable information bits to match the widened knowledge bus. Because to the everyday options of CMOS technology, for integration advanced systems in tiny silicon area with fairly low power dissipation at speeds demanded by most of the applications, CMOS VLSI has been the apparent selection of designers. The overall electronic systems use CMOS technology at the rear finish. To accomplish high-density chip, ultra-low power dissipation, and high performance, complementary metal oxide semiconductor (CMOS) devices are scaled since last 30 years. As a result, the propagation delay time has been reduced by half-hour per technology resulting in the silicon chip performance being doubled each 2 years. Scaled technology has reduced the availability voltage to get low power consumption [1, 2, 3]. SRAM occupies most of the system on chip (SoC) space and dominates the system performance and power. Particularly in bioelectronics and alternative emerging applications, low provide voltage and low-power SRAMs are needed to increase system operation with restricted energy resource. Therefore, design of low-voltage and low-power sub threshold SRAM circuit [4] Cell has three completely different states:

Standby (Idle circuit): If the word line isn't active then M5 and M6 disconnect the cell from the bit lines and therefore the two cross coupled inverter can still reinforce one another as long as they're connected to the availability.

Reading (Data has been requested): It entirely depends on pre-charging conception, as each the bit-lines and word line are active high. generally tiny low delta delay is occurred across the bit-lines which is able to resolved by attaching a way electronic equipment at the tip of the cell. The upper the sensitivity of sense electronic equipment, the quicker the speed of browse operation.

Writing: change the contents regardless of the worth we wish to written same value is applied to the bit-lines. Bit-line input drivers are designed to be abundant stronger than the comparatively weak transistors within the cell itself, in order that they'll simply override the previous state of the cross coupled inverters. Careful size of the transistors in an SRAM is required to make sure correct operation [5].

II. LITERATURE SURVEY

Liu et al. [6]. Introduce 9T SRAM is shown in Fig.4 Write occurs just as in the 6T SRAM cell. Reading occurs

separately through N5, N6 and N7 controlled by the read signal going high. This design has the problem of the high bit line capacitance with more pass transistors on the bit line.

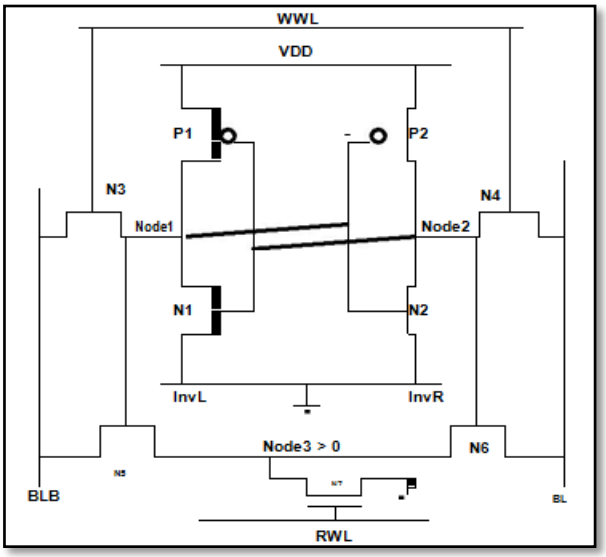

Figure 1: 9T SRAM Cell Structure

A Jain et al. [7]. Proposed three techniques i.e. MT-CMOS (Multi- Threshold CMOS), Dynamic Voltage Scaling and Gated Voltage Technique in 90nm CMOS technology using Cadence Virtuoso to reduce leakage power in 6T and 5T SRAM cell. By performing proper read and write operations, leakage current was calculated. Subsequently leakage reduction technique was applied and found that MT-CMOS technique is best. The leakage power in 6T SRAM cell was reduced to 46% and in 5T SRAM cell 43.71%.

K Rathi et al. [8].Analyzed 8T Static Random Access Memory cell at 65nm process technology is shown in fig.3 this topology was originally proposed for a subthershold static RAM design and optimized for functionality and performance over a large voltage rang. A write operation is performed through WWL, WBL and WBLX port, where as single ended read operation is exercised through RWL and RBL ports.RBL is precharged at the end of each read cycle and keeps precharged during a write cycle. In this bit cell write and read ports are decoupled in contrast to the traditional 6T cell. Read-SNM problem is eliminated and 6T static RAM part can be sized for better writeablity without trading off RSNM. This makes the voltage drop across unaccessed read buffers zero and hence leakage on read bit line is highly reduced. Vdd is the virtual supply nodes for the cross coupled inverters and its voltage can be brought down during a write access to weaken PMOS load device and ease write ability problem at low voltage. Since the entire bit cells on a row are written and read at the same time, Vdd is shared across one row of memory cells.

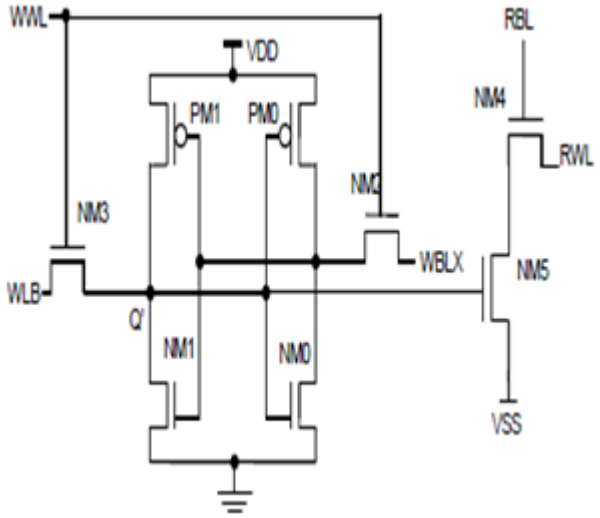

Figure2:8T SRAM cell Structure

S Hollis et al [9]. Proposed a novel 6T SRAM cell for ultra low-voltage applications. Author found 36% improvement as compared to conventional 6T SRAMs. Moving from 130nm to 65nm technology area increased from 71% to 82%. Leakage power was reduced up to 21%. The whole work was done in 65nm technology.

Abhijeet et al [10] proposed Dual Vth 5T SRAM cell and compared to dual Vth 6T SRAM cell using 180nm CMOS technology. The leakage current for 5T SRAM cell was found to be 210mu watt and for 6T SRAM cell was found to be 390mu watt. Write delay for “0” and “1” was calculated to be 3.0038e-8ns and 1.53e-8ns respectively for 5T and 3.05e-8ns and 1.51e-8ns respectively for 6T.

R.K. Chauhan et al [11] reported 7T, 6T, 5T and 4T cells configuration and found the highest stability in 6T SRAM cell. The process was carried out using 32nm technology. The whole circuit verification was done using Tanner tool, design schematic on S-Edit and net list simulation was done using T-spice. Finally, waveforms were analyzed through W-Edit. An asymmetric configuration was implemented to reduce leakage power and found 6T SRAM best. Power dissipation in 6T SRAM cell for standby, reading and writing mode was found to be 8.2e-11, 4.5e-7 and 5.23e-11 respectively. Delay calculated for read and write was 25ns and 0.8ns respectively.

K. Harikishore et al [12] proposed an 8-bit 6T SRAM cell with Low Sub threshold leakage power using leakage current reduction technique. The circuit was designed using 180nm CMOS/ VLSI technology in Micro-wind tool and

found 50% less power consumption than conventional 6T SRAM.

Pankaj Agarwal et al,[13].existing SRAM Cells 6T SRAM Cell A SRAM cell should perform read , write and hold operations as long as the power is applied. An ordinary flip-flop could accomplish this requirement, but the size is quite large. This is a good trade-off in large RAM arrays where the memory cells dominate the area. This smaller cell size offers shorter wires and therefore it results in lower dynamic power consumption. The 6T SRAM cell contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. The 6T SRAM cell achieves its compactness for reading and writing the cell. The positive feedback corrects disturbances caused by leakage or noise

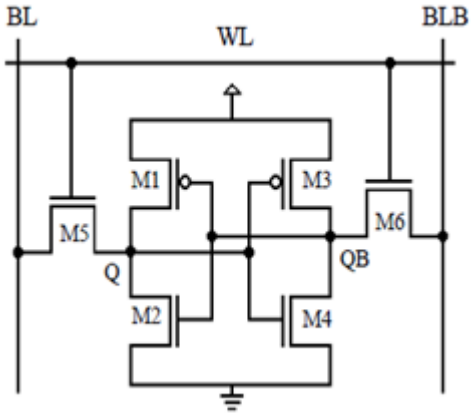

Figure 3. 6T-SRAM bit-cell.

6T SRAM cell each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, or more transistors per bit. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected, to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows.

Problem IN SRAM: in research in SRAM have become a critical component of many VLSI chips more power consumption. In circuit 6T SRAM cell problem are more power consumption in Write operation in CMOS SRAM cell how many transistors are used in the implementation of SRAM are also optimizing.

Proposed Design: The circuits have been simulated on Micro Wind tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns the consumption of power and speed of SRAMs are some important issues among a number of factors that provides a solution which describes multiple designs that minimize the consumption of power our propose SRAM . An SRAM is designed and how it works is essential to building advanced logic circuits and reduces power consumption and reduces power during the Write operation in CMOS SRAM cell and proposed SRAM cell circuit designed using switching principles. Minimize power consumption.

III. PROJECTED OUTCOME

Minimize power consumption. Designed effective SRAM circuit and enhanced SRAM base low power consumption Best possible answer.

IV. CONCLUSION

In study in area of circuit designed in SRAM cell, The SRAM is designed for high speed operation, with low power technique by using small voltage swings on the bit-lines during write operation. The 16nm-8T format exhibited enormous amount of read stability compared to that of 6T format. Also it was found that the most stable form of 8T-SRAM cell can be designed by keeping the cell ratio as minimum as unit of power. Standby leakage power dissipation by the cell was estimated at different sizing of the transistors. It is almost equal to 6T SRAM write delay and 8T. The 9T SRAM structure uses the advantages of 6T and 8T SRAM, 9T SRAM uses the two bit lines and also have the different read and write line. Our proposed designed effective SRAM circuit and enhanced SRAM base low power consumption.

REFERENCES

[1]. Aur, Y., Member, S., Buchanan, D.A., Chen, W.E.I., Frank, D.J., Ismail, K.E. and Wong, H. (1997) CMOS Scaling into the Nanometer Regime. Proceedings of the IEEE, 85, 486-504.

[2]. Breed A.A. and Roenker, K.P. (2008) Comparison of the Scaling Characteristics of Nanoscale SOI N-Channel Multiple-Gate MOSFETs. Analog Integrated Circuits and Signal Processing, 56, 135-141.

[3]. Foty, D. (1999) Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design. Analog Integrated Circuits and Signal Processing, 21, 229-252.

[4]. I. J. Chang, J. J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T sub threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 650–658, Feb. 2009.

[5]. Shivani Yadav, Neha Malik, Ashutosh Gupta and Sachin Rajput, "Low Power SRAM Design with Reduced Read/Write Time", International Journal of Information and Computation Technology, ISSN 0974-2239 Volume 3, Number 3, pp. 195-200, 2013.

[6]. Liu Z, Kursun V. Characterization of a novel nine-transistor SRAM cell. IEEE Trans Very Large Scale Integr (VLSI) Syst, 16:488–92. No. 4, 2008.

[7]. Anupriya Jain, "Analysis and Comparison of Leakage Reduction Techniques for 6T SRAM and 5TSRAM in 90nm Technology", International Journal of Engineering Research & Technology (IJERT), Vol. 1 Issue 6, August – 2012, ISSN: 2278-0181

[8]. Shilpi Birla, Neeraj Kumar Shukla, Kapil Rathi, Rakesh Kumar Singh, Manisha Pattanaik,"Analysis of 8T SRAM Cell at Various Process Corners at 65 nm Process Technology," Circuits and Systems, pp.326-329, 2011.

[9]. Jawar Singh, Dhiraj K. Pradhan, Simon Hollis and Sarju P. Monahy, "A single ended 6T SRAM cell design for ultra-low-voltage applications", IEICE Electronics Express, Vol.5, No.18 .

[10]. Chetna, Abhijeet, "Design of Low Power 5TDual Vth SRAM-Cell", IOSR Journal of Engineering May. 2012, Vol. 2(5) pp: 1128-1132

[11]. R.K. Chauhan, Sushil Kumar Gupta, "Low- Power Analysis of Various 1-bit Sram Cells Using Spice", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 2, Issue 8, August 2013, ISSN: 2278 – 909X.

[12]. K. Harikishore, Atluri Jhansi Rani, Fazal Noor Basha, V. G. Santhi Swaroop, L. VeeraRaju, "Designing and Analysis of 8 Bit SRAM Cell with Low Sub threshold Leakage Power", International Journal of Modern Engineering Research (IJMER) www.ijmer.com Vol.2, Issue.3, May-June 2012 pp733-741 ISSN: 2249-6645.

[13]. Pankaj Agarwal, Sanjeev K. Jain, "A Low Leakage and SNM Free SRAM Cell Design in Deep Sub micron CMOS Technology "Proceedings of the 19th International Conference on VLSI Design (VLSID'06), 2006.

[14]. Shigeki Ohbayashi, Makoto Yabuuchi, .Koji Niiand, Susumu Imaoka "A 65-nm SoC Embedded 6T-SRAM Designed for Manufacturability With Read and Write Operation Stabilizing Circuits" IEEE journal of solid-state circuits, Vol. 42,April 2007, pp820 -829

[15]. Rajasekhar Keerthi and Chein-in Henry Chen "Stability and Static Noise Margin Analysis of Low-Power SRAM" I2MTC 2008 – IEEE International Instrumentation and Measurement Technology Conference, Victoria, Vancouver Island, Canada, May 12-15, 2008.